Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 71671

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2017.

Second Semester

Computer Science and Engineering

CS 6201 — DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to Information Technology)

(Regulations 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Classify the logic families by its operations.
2. State and prove the consensus theorem.
3. What is priority encoder?
4. Draw the circuit for 2-to-1 line multiplexer.
5. What are the significances of state assignment?
6. Write any two applications of shift register.
7. Define race around condition.
8. What is edge triggered flip flop?
9. List the major differences between PLA and PAL.
10. What is memory decoding?

PART B — (5 × 16 = 80 marks)

11. (a) Using Tabulation method simplify the Boolean function $F(w,x,y,z) = \sum(1,2,3,5,9,12,14,15)$ which has the don't care conditions $d(4,8,11)$. (16)

Or

(b) Simplify the following expression :

$y = m_1 + m_3 + m_4 + m_7 + m_8 + m_9 + m_{10} + m_{11} + m_{12} + m_{14}$ using

(i) Karnaugh Map

(ii) Quine McClusky method. (16)

12. (a) Construct a BCD adder circuit and write a HDL program module for the same. (16)

Or

(b) Implement the Boolean function using 8:1 multiplexer F(W,X,Y,Z) = W'XZ'+ WYZ + X'YZ + W'Y'Z. (16)

13. (a) Implement T-flip flop and JK flip flop using D flip flop. (16)

Or

(b) Design and implement Mod-5 Synchronous Counter using JK flip flop and also draw the timing diagram. (16)

14. (a) Summarize the design procedure for asynchronous sequential circuit. (16)

Or

(b) Explain the different types of hazards that occurs in asynchronous sequential circuits and Combinational circuits. (16)

15. (a) Design a 16 bit RAM array (4 × 4 RAM) and explain the operation. (16)

Or

(b) Explain the following :

(i) ASIC (8)

(ii) Field Programmable Gate Array. (8)

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