Question Paper Code : 97046

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2014.

Third Semester

Computer Science and Engineering

CS 6303 — COMPUTER ARCHITECTURE

(Common to Information Technology)

(Regulation 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. State Amdahl's Law.

2. Brief about Relative addressing mode with an example.

3. Define Little Endian arrangement.

4. What is DMA?

5. What is the need for Speculation?

6. What is Exception?

7. What is Flynn's Classification?

8. Brief about Multithreading.

9. Differentiate Programmed I/O and Interrupt I/O.

10. What is the purpose of Dirty/Modified bit in Cache memory?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Assume a two address format specified as source, destination. Examine the following sequence of instructions and explain the addressing modes used and the operation done in every instruction. (10)

(1) Move (R5)+, R0

(2) Add (R5)+, R0

(3) Move R0, (R5)

(4) Move 16(R5), R3

(5) Add #40,R5.

(ii) Consider the computer with three instruction classes and CPI measurements as given below and Instruction counts for each instruction class for the same program from two different compilers are given. Assume that the computer's clock rate is 4GHZ.Which Code sequence will execute faster according to execution time? (6)

Code from	CPI for this Instruction Class		
	A	B	C
CPI	1	2	3
Code from	Instruction Count for each Class		
	A	B	C
Compiler 1	2	1	2
Compiler 2	4	1	1

Or

(b) (i) Explain the components of a computer System. (8)

(ii) State the CPU performance equation and discuss the factors that affect performance. (8)

12. (a) (i) Multiply the following pair of signed nos. using Booth's bit-pair recoding of the multiplier. A = +13 (Multiplicand) and B = -6 (Multiplier). (10)

(ii) Briefly Explain Carry lookahead adder. (6)

Or

(b) Divide $(12)_{10}$ by $(3)_{10}$ using the Restoring and Non restoring division algorithm with step by step intermediate results and explain. (16)

13. (a) Explain Data path and its control in detail. (16)

Or

(b) What is Hazard? Explain its types with suitable examples. (16)

14. (a) Explain Instruction level Parallel Processing. State the challenges of parallel Processing. (16)

Or

(b) Explain the terms:

(i) Multicore Processor.

(ii) Hardware Multithreading. (16)

15. (a) (i) Explain mapping functions in cache memory to determine how memory blocks are placed in Cache. (8)

(ii) Explain in detail about the Bus Arbitration techniques in DMA. (8)

Or

(b) (i) Draw different memory address layouts and brief about the technique used to increase the average rate of fetching words from the main memory. (8)

(ii) Explain in detail about any two Standard Input and Output Interfaces required to connect the I/O device to the Bus. (8)