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Question Paper Code : 90155

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2019
Fourth/Fifth Semester
Computer Science and Engineering
CS8491 – COMPUTER ARCHITECTURE
(Common to : Robotics and Automation Engineering/Computer and Communication
Engineering/Information Technology)
(Regulations 2017)

Time : Three Hours

Maximum : 100 Marks

Answer ALL questions

PART – A

(10×2=20 Marks)

1. What is register indirect addressing mode ? When it is used ?
2. Define word length.
3. What is half adder ?
4. What are the main features of Booth's algorithm ?
5. Define datapath in the processor unit.
6. What is the role of cache memory in pipeline ?
7. What do you mean by static memories ?
8. Define Hit and Miss in cache.
9. What is Flynn's classification ?
10. What are the properties of Multi-Core Systems ?

PART – B

(5×13=65 Marks)

11. a) Explain in detail the various components of computer system with neat diagram.

(OR)

- b) Mr. Thomas has got a new laptop, at memory address 101 Add A, B instruction is residing. How will the processor fetch the instruction from the memory and execute the instruction based on various registers in the CPU. Also draw the architectural diagram for the above scenario.

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12. a) Mr. John has been assigned a project by his Team Leader in ALS Technologies. His project is to design an algorithm for two's complement division using addition and subtraction operations. Help Mr. John in designing an algorithm by sketching the flowchart for restoring division and also check the working of it with the following numbers : $21 \div 4$.

(OR)

- b) Mr. David is Processor Designer at IBM and he is visiting your college for an internship interview. During the interview Mr. David asks you to sketch the flow chart for floating point multiplication and also check the working of it with the following numbers : $X = 4.5_{(10)}$ and $Y = 11.25_{(10)}$. Provide an appropriate solution.

13. a) Explain data path and its control in detail.

(OR)

- b) What is pipelining ? Discuss about pipelined data path control.

14. a) Discuss about SISD, MIMD, SIMD, SPMD and vector systems.

(OR)

- b) What is hardware multithreading ? Compare and contrast fine grained multi-threading and coarse grained multi-threading.

15. a) Consider a cache of 256 blocks in size, each block has 2^4 words. The main memory size is 2^{12} blocks, each block has 2^4 words. How many bits are required for each of the TAG, SET/BLOCK and WORD FIELDS for different mapping techniques ? Wherever needed assume that there are 8 ways in each set.

(OR)

- b) Consider a system which transfers 2 MB file from memory to pendrive.

- i) If memory is using Handshaking Protocol to send the file, depict clearly how the data transfer takes place in case of source initiated and destination initiated data transfer. (7)

- ii) When the file is being transferred there should be minimal intervention of the processor. Suggest a suitable technique for the above operation and explain it with proper justification and diagrams. (6)

PART - C

(1×15=15 Marks)

16. a) What is an addressing mode ? Explain the various addressing modes with suitable examples.

(OR)

- b) Explain in detail about centralized shared memory and distributed memory multiprocessor.
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