

Reg. No. 9 2 0 2 1 4 1 0 4 0 0 1

Question Paper Code : 57241

B.E/B.Tech. DEGREE EXAMINATION, MAY/JUNE 2016

Sixth Semester

Electronics and Communication Engineering

CS 6303 – COMPUTER ARCHITECTURE

(Common to Information Technology)

(And also common to Fifth Semester Elective – Electronics and Instrumentation Engineering, Instrumentation and Control Engineering, Fifth Semester – Robotics and Automation Engineering and Third Semester Computer Science and Engineering)

(Regulations 2013)

Time : Three Hours

Maximum : 100 Marks

Answer ALL questions.

PART – A (10 × 2 = 20 Marks)

1. How to represent Instruction in a Computer System ?
2. Distinguish between auto increment and auto decrement addressing mode.
3. Define ALU.
4. What is Subword Parallelism ?
5. What are the advantages of pipelining ?
6. What is Exception ?
7. State the need for Instruction Level parallelism.
8. What is Fine grained Multithreading ?
9. Define Memory hierarchy.
10. State the advantages of virtual memory.

PART - B (5 × 16 = 80 Marks)

11. (a) Discuss about the various components of a computer system. (16)

OR

- (b) Elaborate the different types of addressing modes with a suitable example. (16)

12. (a) Explain briefly about floating point addition and Subtraction algorithms. (16)

OR

- (b) Define Booth Multiplication algorithm with suitable example. (16)

13. (a) What is pipelining ? Discuss about pipelined data path and control. (16)

OR

- (b) Briefly explain about various categories of hazards with examples. (16)

14. (a) Explain in detail about Flynn's classification. (16)

OR

- (b) Write short notes on : (16)

- (i) Hardware multithreading
- (ii) Multicore processors.

15. (a) Define Cache Memory ? Explain the Various Mapping Techniques associated with cache memories. (16)

OR

- (b) Explain about DMA controller, with the help of a block diagram. (16)

16/3/2021
Dr. C. JEGADHEESAN
PRINCIPAL
Ghadrana College of Engineering & Technology,
PULIYUR - CF., KARUR (Dt.) - 629 114.