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B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2019.

Third/Fifth/Sixth Semester

Computer Science and Engineering

CS 6303 – COMPUTER ARCHITECTURE

(Common to: Electronics and Communication Engineering/Electronics and Communication Engineering/Electronics and Instrumentation Engineering/Instrumentation and Control Engineering/Robotics and Automation Engineering /Information Technology)

(Regulation 2013)

Also common to PTCS 6303 – Computer Architecture for Computer Science and Engineering (Fifth Semester – Regulation 2014)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Write the components of a computer system and list their functions.
2. Give the MIPS code for the statement f = (g + h) - (i + j).
3. State the rules to add two integers.
4. Define scientific notation and normalized notation.
5. Define edge triggered clocking.
6. Identify the hazards with respect to a processor function.
7. Neatly sketch the three primary units of dynamically scheduled pipeline.
8. Define speculation with example.
9. What is miss penalty?
10. How many total bits are required for a direct-mapped cache with 16 KB of data and 4-word blocks, assuming a 32-bit address?

PART B — ($5 \times 13 = 65$ marks)

11. (a) Explain how performance is calculated in a computer system and derive the necessary performance equations.

Or

(b) Explain how instructions that involve decision making are executed with an example.

12. (a) Discuss how ALU performs division with the flow chart and the block diagram.

Or

(b) Explain floating point addition with a neat block diagram of ALU unit.

13. (a) Explain the process of building a single data–path with a neat diagram.

Or

(b) Explain data hazards and stalls with neat diagrams and suitable examples.

14. (a) Explain Flynn's classification with neat diagrams.

Or

(b) Explain hardware multithreading with neat diagrams.

15. (a) Explain the process of measuring the performance of cache memory with required metrics?

Or

(b) Explain the virtual memory organization followed in digital computers.

PART C — ($1 \times 15 = 15$ marks)

16. (a) (i) Assume a two address format specified as source, destination. Examine the following sequence of instructions and explain the addressing modes used and the operation done in every instruction.

(1) Move (R5)+,R0

(2) ADD (R5)+,R0

(3) MOVE RO, (R5)

(4) Move 16(R5), R3

(5) Add #40, R5 (5)

(ii) Consider the following code segment in C:

```
a = b + e;
c = b + f;
```

Here is the generated MIPS code for this segment, assuming all variables are in memory and are addressable as off sets from $t0:

```
lw   $t1,  0($t0)
lw   $t2,  4($t0)
add  $t3,  $t1,$t2
sw   $t3,  12($t0)
lw   $t4,  8($t0)
add  $t5,  $t1,$t4
sw   $t5,  16($t0).
```

Find the hazards in the preceding code segment and reorder the instructions to avoid any pipeline stalls? (10)

Or

(b) (i) Analyze the merits and demerits of microprogrammed control over hardwired control. (7)

(ii) Analyze and tabulate the major features of programmed I/O, DMA and interrupts. (8)