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Question Paper Code : 50418

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2017

Seventh Semester

Electronics and Communication Engineering

EC 6009 – ADVANCED COMPUTER ARCHITECTURE

(Regulations 2013)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. State Amdahl's law.
2. If a 20% reduction in voltage leads to 15% reduction in frequency, what would be the impact on dynamic energy and power ?
3. What is a reorder buffer ?
4. What is meant by delayed branching ?
5. Use GCD test to identify if loop-carried dependency exists for the following loop :

   for (i = 1; i < = 100; i ++) {

   A[3*i + 5] = A [5*i + 8]*7;

   }
6. How did single core architectures exploit data level parallelism ?
7. What is meant by sequential consistency ?
8. What is meant by false sharing ?
9. Define the terms reliability and availability.
10. Point out one simple technique used to reduce each of the three "C" misses in cache memories.

PART – B (5×16=80 Marks)

11. a) i) Discuss the factors that need to be considered while designing the Instruction Set Architecture of a processor. (10)

ii) What are the various performance measures available to evaluate the performance of processors ? How do each of these relate to the ultimate measure of performance ? Explain. (6)

(OR)

b) i) What are the major concerns that should be addressed by a system architect with respect to power and energy ? Discuss the techniques that are commonly employed to address these issues. (10)

ii) What are the different classes of parallelism and parallel architectures that are available ? (6)

12. a) i) Consider the following code :

```
Loop :  L.D.     F2, 0(R1)
        MUL.D    F4, F2, F0
        L.D.     F6, 0(R2)
        ADD.D    F6, F4, F6
        S.D.     0(R2), F6
        DADDIU   R1, R1, #8
        DADDIU   R2, R2, #8
        CMPI     R3, R1, # 800
        BEQZ     R3, loop
```

Assume that there are separate functional units for effective address calculations, for ALU operations and for branch condition evaluation. Assume latencies of 3 for Add and 5 for Multiply. Assume that loads and stores access memory one clock cycle after the effective address calculation. Show the working of this code for two iterations of the loop when executed on a single issue Tomasulo processor that supports speculation. (10)

ii) Write a short note on the different types of multiple issue processors. (6)

(OR)

b) i) Discuss the various hardware techniques used for handling control hazards. (10)

ii) What is meant by loop unrolling ? Discuss its advantages and disadvantages. (6)

13. a) i) Discuss the salient features of vector processors. **(10)**

ii) How do you determine the execution time of a sequence of vector operations ? Explain with an example. **(6)**

(OR)

b) i) What are the architectural features that distinguish a GPU from a normal CPU ? Discuss with a case study. **(10)**

ii) Identify the true dependences, output dependences and anti dependences in the code given below and eliminate the name dependences through register renaming. **(6)**

```
for (i = 0; i < 100; i = i + 1) {
Y[i] = X[i]/c;/*S1*/
X[i]  = X[i] + c; /* S2*/
Z[i] = Y[i] + c; /*S3*/
Y[i] = c – Y[i];/* S4*/
}
```

14. a) i) Discuss the salient features of the Intel i7 processor. **(10)**

ii) Explain the concept of Simultaneous Multi Threading. **(6)**

(OR)

b) i) Explain the snoop based cache coherence protocol with a state diagram. **(10)**

ii) How are spin locks implemented using cache coherence ? **(6)**

15. a) i) Discuss any five advanced cache optimization techniques and point out the factors that get optimized. **(10)**

ii) Suppose that in 1000 memory references there are 50 misses in the first-level cache and 20 misses in the second-level cache. What are the various miss rates ?

Assume the miss penalty from the L2 cache to memory is 100 clock cycles, the hit time of the L2 cache is 10 clock cycles, the hit time of L1 is 1 clock cycle and there are 2 memory references per instruction. What is the average memory access time ? **(6)**

(OR)

b) i) Discuss the concept of virtual memory and explain how a virtual memory system is implemented, pointing out the hardware and software support. **(10)**

ii) Discuss the different levels of RAID technology, listing their advantages and disadvantages. **(6)**

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