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Question Paper Code : 27206

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2015.

Third Semester

Electrical and Electronics Engineering

EE 6301 — DIGITAL LOGIC CIRCUITS

(Common to Electronics and Instrumentation Engineering and Instrumentation and Control Engineering)

(Regulations 2013)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is an unit distance code? Give an example.
2. Define Fan-out.
3. Convert the given expression in canonical SOP form $Y = AB + A'C + BC'$.
4. Draw the logical diagram of EX-OR gate using NAND gates.
5. Draw the truth table and state diagram of SR flip-flop.
6. What is edge triggered flip flops?
7. What is PROM?
8. Compare pulsed mode and fundamental mode asynchronous circuit
9. Write the behavioral model of D flip flop.
10. List out the operators present in VHDL.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Draw the CMOS logic circuit for NOR gate and explain its operation. (8)
(ii) Perform the following operation $(756)_8 - (437)_8 + (725)_{16}$. Express the answer in octal form. (8)

Or

- (b) (i) A 12 bit Hamming code word containing 8 bits of data and 4 parity bits is read from memory. What was the original 8 bit data word that was written into memory if the 12 bit word read out is as (1) 101110010100 and (2) 111111110100. (12)
- (ii) Briefly discuss weighted Binary code. (4)
12. (a) (i) Simplify the boolean function using K-map and implement using only NAND gates.

$$F(A, B, C, D) = \sum m(0, 8, 11, 12, 15) + \sum d(1, 2, 4, 7, 10, 14).$$
Mark the essential and non-essential prime implicants. (8)
- (ii) Design a full subtractor and implement using logic gates. (8)
- Or
- (b) (i) Design a 4 bit BCD to excess 3 code converter and implement using logic gates. (8)
- (ii) What is a multiplexer? Implement the following Boolean function with 8×1 MUX and external gates

$$F(A, B, C, D) = \sum m(1, 3, 4, 11, 12, 13, 14, 15).$$
 (8)
13. (a) (i) A sequential circuit with two D flip flops A and B, input X and output Y is specified by the following next state and output equations

$$A(t+1) = AX + BX,$$

$$B(t+1) = A'X$$

$$Y = (A + B)X'.$$
Draw the logic diagram, derive state table and state diagram. (12)
- (ii) Realize T flip-flop using JK flip-flop. (4)
- Or
- (b) (i) Design a synchronous decade counter using T flip flop and construct the timing diagram (8)
- (ii) Design a mealy model of sequence detector to detect the pattern 1001. (8)
14. (a) Design an asynchronous sequential circuit (with detailed steps involved) that has 2 inputs x_1 and x_2 and one output z. The circuit is required to give an output $z = 1$ when $x_1 = 1$, $x_2 = 1$ and $x_1 = 1$ being first. (16)
- Or
- (b) Show how to program the fusible links to get a 4 bit Gray code from the binary inputs using PLA and PAL and compare the design requirements with PROM. (16)
15. (a) (i) Write a VHDL program for 1 to 4 Demux using dataflow modelling. (8)
- (ii) Write a VHDL program for Full adder using structural modelling. (8)
- Or
- (b) Explain in detail the RTL design procedure. (16)