Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 90194

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2019

Third Semester

Electrical and Electronics Engineering

EE 8351 – DIGITAL LOGIC CIRCUITS

Common to : Electronics and Instrumentation Engineering/Instrumentation and Control Engineering

(Regulations 2017)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A (10×2=20 Marks)

1. List the different types of output configuration in TTL.
2. Given the two binary numbers X = 1010100 and Y = 1000011, perform subtraction (a) X – Y and (b) Y – X using 2's-complements.
3. Write the difference between sequential and combinational circuits.
4. Draw basic configuration of three PLDs.
5. Mention the role of master clock generator in synchronous circuits.
6. Define state assignment.
7. Name the three types of hazards.
8. Define synchronous sequential circuit.
9. Mention the languages that are combined together to get VHDL language.
10. Expand the T'Base and T'Low predefined attributes.

PART – B (5×13=65 Marks)

11. a) Explain the two types of MOS families. (13)

(OR)

b) With the neat circuit diagram, explain the operation of ECL. (13)

12. a) Simplify the following expressions in (1) sum of products and (2) products of sums

a) $x'z' + y'z' + yz' + xy$ (4)

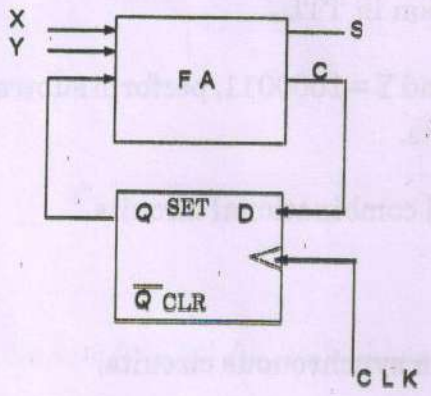
b) $AC' + B'D + A'CD + ABCD$ (4)

c) $(A' + B' + D')(A + B' + C')(A' + B + D')(B + C' + D')$ (5)

(OR)

b) Design a half subtractor circuit with inputs x and y and outputs D and B. The circuit subtracts the bits x-y and places the difference in D and the borrow in B. (13)

13. a) A sequential circuit has one flip-flop Q, two inputs x and y and one output S. It consists of a full-adder circuit connected to a D flip-flop, as shown in figure. Derive the state table and state diagram of the sequential circuit. (13)



(OR)

b) Draw and explain the operation of a JK and master slave JK flip flop. (13)

14. a) Discuss about the hazards in asynchronous sequential circuits and the methods to eliminate them. (13)

(OR)

b) Describe the effect of races in asynchronous sequential circuit design. (13)

15. a) Develop a VHDL code to realize a 3 bit Gray code counter using case statement. **(13)**

(OR)

b) Discuss briefly the operators and packages in VHDL. **(13)**

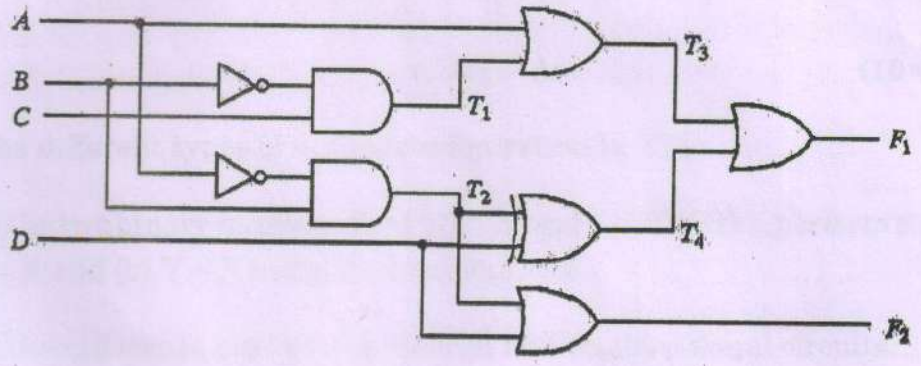
PART – C **(1×15=15 Marks)**

16. a) Consider the combinational circuit shown in Fig. **(15)**

i) Derive the Boolean expressions for T_1 through T_4. Evaluate the outputs of F_1 and F_2 as a function of the four inputs.

ii) List the truth table with 16 binary combinations of the four inputs variables. Then list the binary values for T_1 through T_4 and outputs F_1 and F_2 in the table.

iii) Plot the output Boolean functions obtained in part (b) on maps and show that the simplified Boolean expressions are equivalent to the ones obtained in part (a).



(OR)

b) Implement the following function using PLA and PAL: $F_1(A,B,C) = \Sigma m(3,5,6,7)$ and $F_2(A, B, C) = \Sigma m(0,2,4,7)$. **(15)**