Chettinad
College of Engineering & Technology
Approved by AICTE-New Delhi and Affiliated to Anna University-Chennai.

DEPARTMENT OF ECE

E-CHRONICA 2025

MAGAZINE

NH-67, Karur – Trichy Highway, Puliyur CF, Karur, Tamilnadu – 639114.

https://chettinadtech.ac.in/index.php

TABLE OF CONTENT

HoD'S DESK

Dear Students, Faculty, and Readers,

It is with great pleasure that I extend my warm greetings to you through this edition of our E-Chronica magazine. Our department has been making remarkable strides in academics. Students have interests in various technical competitions, faculty members have contributed to the projects and activity based learning.

Looking ahead, we aim to introduce more hands-on learning opportunities, strengthen our research initiatives, and encourage students to take up innovative projects. I urge every student to explore beyond textbooks, engage in interdisciplinary learning, and build problem-solving skills. Our faculty continues to be the backbone of this growth, and I sincerely appreciate their unwavering dedication.

I am confident that, with our collective efforts, we will continue to achieve new milestones. I extend my gratitude to the editorial team and all contributors who made this magazine possible.

Wishing you all success in your academic and professional journeys! – Dr.M.Kumar, HoD/ECE

ABOUT THE DEPARTMENT

The Department of Electronics and Communication Engineering was established in the year 2007.The department has an intake of 60 students in B.E. course. The department possesses the most advanced equipment in its laboratories. It also provides opportunities to grow and excel in the technical world by conducting regular workshops and programs in various fields. The department is highly active in research work in the fields of broadband communications, VLSI Design, image processing etc. The students are provided adequate training in the field of signal processing, image processing and digital communication. Students are highly motivated to attend in-plant training in some of the most prestigious organizations during their time with the institution.

VISION

- To provide the quality education in the field of Electronics and Communication Engineering which caters the needs of the society in line with the technological revolution

MISSION

- To upgrade the technical knowledge of the students continuously by providing industrial exposure and innovative projects
- To establish a creative learning environment for the students by active learning of the techniques in the electronics and communication engineering field
- To nurture career improvement by facilitating skill development and training in the recent technologies

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

- To provide the students with a strong foundation in the required sciences in order to pursue studies in Electronics and Communication Engineering
- To gain adequate knowledge to become good professional in electronics and communication engineering associated industries, higher education and research
- To develop attitude in lifelong learning, applying and adapting new ideas and technologies as their field evolves
- To prepare students to critically analyze existing literature in an area of specialization and ethically develop innovative and research oriented methodologies to solve the problems identified
- To inculcate in the students a professional and ethical attitude and an ability to visualize the engineering issues in a broader social context

PROGRAM SPECIFIC OUTCOMES (PSOs)

- PSO1: Design, develop and analyze electronic systems through application of relevant electronics, mathematics and engineering principles
- PSO2: Design, develop and analyze communication systems through application of fundamentals from communication principles, signal processing, and RF System Design & Electromagnetics
- PSO3: Adapt to emerging electronics and communication technologies and develop innovative solutions for existing and newer problems

ECE TOPPER'S - NOV-DEC 2023

II Year ECE		III Year ECE		IV Year ECE	
Name	CGPA	Name	CGPA	Name	CGPA
Srimathi M	**9.16**	Dharani K	**8.63**	Divya K	**8.5**
Jothika G	**8.93**	Yuvashree N	**8.58**	Varni S	**8.42**
Hiriseeka N	**8.79**	Pooja H	**8.46**	Bubalakannan R	**8.19**

STUDENT'S FOLIO

Data Encoding Techniques to Improve the Performance of SoC A Comparative Analysis of OEFNSC Encoding with and Without Clock Gating - P. Abisekar, S. Santhanabharathi, T. Sivatamil, P. Satheesh from 3rd year ECE

ABSTRACT

This paper presents a comprehensive study on the application of clock gating techniques to the Odd-Even-Full-Normal inversion considering the total Self and Coupling switching activity (OEFNSC) encoding scheme in System-on-Chip (SoC) designs. We analyze the impact of clock gating on power consumption, performance, and area overhead in OEFNSC-based interconnect systems. Our results demonstrate significant improvements in energy efficiency with minimal impact on performance when clock gating is applied to OEFNSC encoding. Detailed comparisons between OEFNSC implementations with and without clock gating across various data widths (8-bit, 16-bit, 32-bit, and 64-bit) and traffic patterns are provided. The findings show that clock-gated OEFNSC achieves up to 30% reduction in dynamic power consumption compared to non-gated OEFNSC, with an average improvement of 22% across all test scenarios. Performance overhead is limited to less than 5% in worst-case scenarios, while area overhead remains below 10%. These results offer valuable insights into optimal design choices for low-power SoC interconnects, particularly in applications where energy efficiency is paramount.

I. INTRODUCTION

The continuous scaling of semiconductor technology has led to the integration of increasingly complex systems on a single chip, known as System-on-Chip (SoC) designs. While this integration offers numerous benefits in terms of performance and functionality, it also presents significant challenges in power management and energy efficiency. As the

number of components and the complexity of on-chip communication increase, power consumption has become a critical concern in SoC design

[1] One of the primary sources of power consumption in SoCs is the on-chip interconnect system, which is responsible for data transfer between various components. The power dissipated by these interconnects can account for a substantial portion of the overall chip power budget, sometimes exceeding 50%

[2] This has led to extensive research in low-power encoding techniques for on-chip data transmission. Among these techniques, the Odd-Even-Full-Normal inversion considering the total Self and Coupling switching activity (OEFNSC) encoding scheme has shown promising results in reducing both self and coupling switching activities, which are major contributors to dynamic power consumption in interconnects

[3] OEFNSC works by selectively inverting portions of the data to minimize transitions, thereby reducing power consumption. While OEFNSC has proven effective, there is still room for improvement, particularly in scenarios where not all encoded data needs to be transmitted in every clock cycle. This is where clock gating, a well-established technique for reducing dynamic power consumption in digital circuits, comes into play. Clock gating works by disabling the clock signal to inactive portions of a circuit, thereby preventing unnecessary switching activity and reducing power consumption

[4] The motivation for this study stems from the potential synergy between OEFNSC encoding and clock gating techniques. By applying clock gating to OEFNSC encoders and decoders, we hypothesize that significant additional power savings can be achieved without substantially impacting performance or greatly increasing design complexity.

This paper makes the following key contributions:

1. We present a detailed analysis of the OEFNSC encoding scheme, including its principles, implementation, and effectiveness in reducing switching activity.

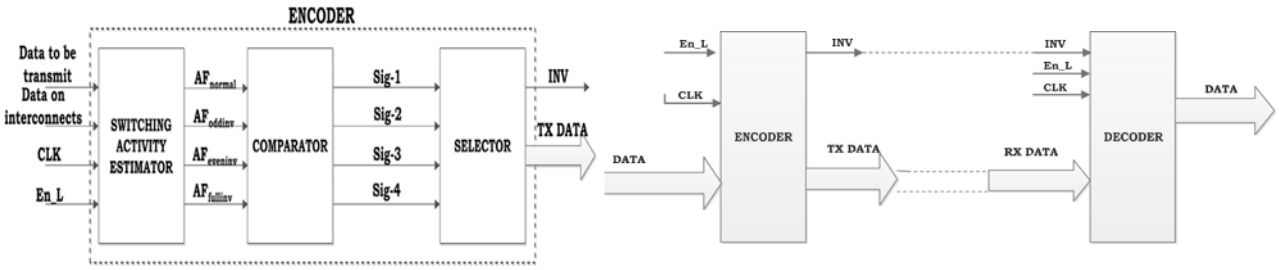
2. We propose and implement a clock-gated version of the OEFNSC encoder and decoder, providing a comprehensive description of the design and implementation process.

3. We run extensive simulation and comparison between OEFNSC implementations with and without clock gating across different data widths (8-bit, 16-bit, 32-bit, and 64-bit) and traffic patterns.

4. We discuss the results of the influence of clock gating on power consumption, performance, and area overhead in OEFNSC-based interconnect systems.

5. We derive insights as well as recommendations for optimal design choices in low-power SoC interconnects based on our research results.

II. OEFNSC ENCODING: PRINCIPLES AND IMPLEMENTATION



Encoder and Decoder

The Odd-Even-Full-Normal inversion considering the total Self and Coupling switching activity (OEFNSC) encoding scheme is designed to minimize both self and coupling switching activities in on-chip interconnects. The algorithm works by selectively inverting portions of the data based on the expected switching activity state.

The OEFNSC algorithm considers four possible encoding options for each data word:

1. Normal (N): The data is transmitted as-is.
2. Odd Invert (OI): Inversion at odd index.
3. Even Invert (EI): Inversion at even index.
4. Full Invert (FI): The inversion of all bits.

- The algorithm, for every data word, computes the expected self-switching activity for all four options and picks out the one with the minimum total switching activity. The self-switching, coupling switching activities are weighted sum as follows:
- Total Switching Activity = α * SS + β * CS
- **P_dyn = 1/2 * (α_S * C_S + α_C * C_C) * V_DD^2 * F_CLK**
- **Where:**
    - α_S is the self-switching activity
    - α_C is the coupling switching activity
    - C_S is the self-capacitance
    - C_C is the coupling capacitance
    - V_DD is the supply voltage
    - F_CLK is the clock frequency
- Data encoding techniques aim to reduce the switching activity (α_S and α_C) to minimize power consumption.
- where α and β are weighing factors whose values can be changed as per an assumed need for an analysis in the importance of self and coupling switching in the target technology.
- The self-switching activity is computed as the number of bit transitions between the current and previous data word. The coupling switching activity is computed based on the transitions of adjacent bits, considering both the current and previous data words.

B. Hardware Architecture

OEFNSC hardware implementation involves the encoder at the receiving end of the interconnect and the decoder at the transmitting end. Fig. 2 illustrates the block diagram of the OEFNSC encoder and decoder. The encoder comprises the following primary components:

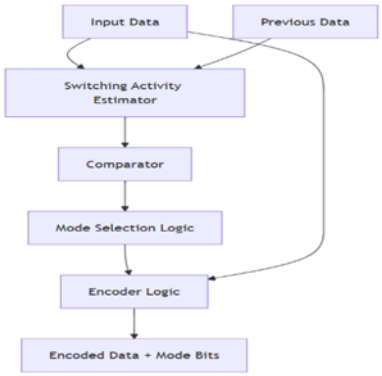
1. Switching Activity Estimator: Computes the expected switching activity for all four encoding options.

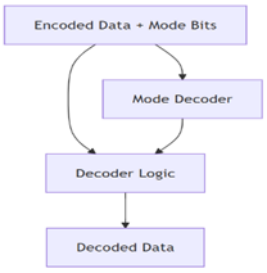
2. Comparator: Determines the encoding mode, which causes minimal switching activity.

3. Encoder Logic: Performs the inversion selected by the comparator.

4. Mode Register: Stores the selected encoding mode, transmitted along with the data.

The decoder is shown in Fig. 2 and is simpler, which consists mainly of decoding logic that performs the reversal based on the received mode bits.





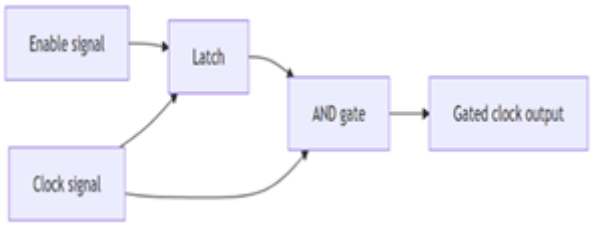
Analysis of Switching Activity Reduction

- The theoretical analysis of the effectiveness of OEFNSC in reducing switching activity can be done. Consider an n-bit data bus. In the worst case, without any encoding, the maximum number of self-transitions per clock cycle is n, and the maximum number of coupling transitions is 2(n-1).
- With OEFNSC encoding, the worst-case scenarios are significantly reduced:
- 1. With self-transitions, the worst scenario is brought down to n/2, because at least n/2 bits are sure not to flip in either OI or EI modes.
- 2. With coupling transitions, the worst scenario is brought down to (n-1), since at any given time bits on either side of each other are unlikely to flip in opposite directions in either OI or EI modes.
- Thus, the overall theoretical switch activity minimization could be achieved with:
- Switching self-reduction: 50%
- Coupling switching reduction: 50%
- In practice, the actual reduction depends on the data patterns and the relative weights assigned to self and coupling switching. Empirical studies have shown average reductions of 30-40% in total switching activity for typical data patterns [3]

III. CLOCK GATING: CONCEPT AND APPLICATION

A. Fundamentals of Clock Gating

Clock gating is a power-saving technique applied to synchronous circuits to reduce dynamic power consumption. The basic principle behind clock gating is to disable the clock signal to portions of a circuit that are not actively computing in a given clock cycle. Clock gating can significantly reduce dynamic power consumption by preventing unnecessary switching of flip-flops and combinational logic. The basic clock gating cell, shown in Fig. 2, consists of a latch and an AND gate. The enable signal determines whether the clock should be passed through to the gated clock output.



B. Types of Clock Gating Techniques

There are several types of clock gating techniques, each with its own trade-offs between power savings, timing impact, and implementation complexity:

1. Latch-based clock gating: Uses a level-sensitive latch to hold the enable signal stable during the active clock edge. This is the most common technique due to its balance of effectiveness and simplicity.
2. Flip-flop based clock gating: Uses an edge-triggered flip-flop instead of a latch. This can provide better timing characteristics but may consume more power than latch-based gating.
3. AND-gate only clock gating: The simplest of them all is the use of an AND gate only, where no latch or flip-flop is used. This type of clock gating is vulnerable to glitches and is typically not recommended for most applications.
4. Multibit clock gating: A clock gate applied to multiple flip-flops or registers minimizes the overhead of clock gating logic.
5. Hierarchical clock gating: Clock gating can be applied at multiple levels in the clock tree, which should result in potentially higher power saving but at an increased complexity.

Even though clock gating can save enormous amounts of power, its realization is not simple and poses some challenges:

1. Timing closure: Clock gating can introduce an additional delay path in the clock tree, possibly leading to violations of timing; hence, thorough analysis and optimization of the clock tree are in order.
2. Glitch prevention: Improper implementation can lead to glitches in the gated clock, causing functional errors. Proper use of latches or flip-flops in the gating cell is crucial.
3. Verification complexity: Clock gating increases the complexity of functional and timing verification, requiring additional test cases and analysis.
4. Tool support: While many EDA tools support clock gating, the quality of results can vary. Designers may need to manually optimize gating insertion in critical paths.
5. Power-up and reset behavior: Special consideration is needed to ensure proper behavior during power-up sequences and system resets.

C. Clock Gating in the Context of Encoding Schemes

Applying clock gating to encoding schemes like OEFNSC presents both opportunities and challenges. The primary opportunity lies in the potential for additional power savings by gating the clock to the encoder and decoder when no new data needs to be processed**.**

However, several factors need to be considered:

1. Enable signal generation: An appropriate enable signal must be derived from the data valid or request signals of the interconnect protocol.
2. Latency impact: Encoding/decoding may be subjected to extra latency due to the clock gating operation, which in turn affects the overall system's timing.
3. Granularity: It will depend on an implementation and a usage pattern on what granularity clock gating should take place: a whole encoder/decoder should be gated or gated separately every individual component.

4. Interaction with encoding logic: Care must be taken to ensure that the clock gating logic does not interfere with the correct operation of the encoding scheme, particularly in maintaining the proper state for calculating switching activity.

In the next section, we will describe our methodology for implementing and evaluating clock gating in the context of OEFNSC encoding.

IV. METHODOLOGY

A. Experimental Setup

To evaluate the effectiveness of applying clock gating to OEFNSC encoding, we conducted a series of experiments using a combination of hardware description language (HDL) simulations and synthesis tools. Our experimental setup consisted of the following components:

Simulation Environment

HDL Simulator: Xilinx Vivado 2018.3

Waveform Analysis: Vivado Simulator (Waveform Viewer)

Synthesis Tools:

Logic Synthesis: Xilinx Vivado Synthesis

Place and Route: Xilinx Vivado Implementation

Technology Libraries:

FPGA Technology: Xilinx FPGA Target Device

Standard cell libraries: Not applicable

B. Implementation Details

We implemented both the standard OEFNSC encoding scheme and a clock-gated version in Verilog HDL. The implementations were parameterized to support data widths of 8, 16, 32, and 64 bits.

1. OEFNSC without Clock Gating:

The standard OEFNSC implementation had the following modules:

1. OEFNSC Encoder
2. OEFNSC Decoder
3. Switching Activity Estimator
4. Mode Selection Logic

2. OEFNSC with Clock Gating:

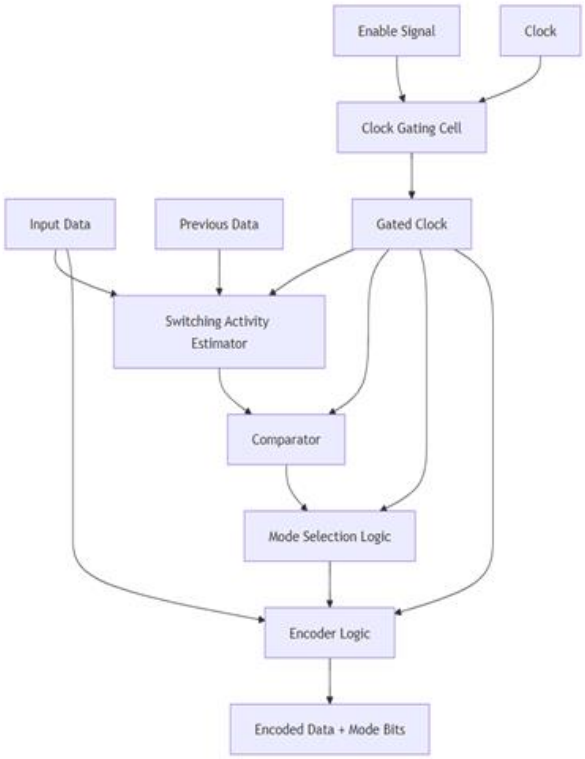
The clock-gated version had the same modules as the standard version, with the addition of:

1. Clock Gating Cells (latch-based)
2. Enable Signal Generation Logic

Clock gating was applied at two levels:

a) Coarse-grained: Gating the entire encoder/decoder when no new data is present

b) Fine-grained: Gating individual components within the encoder/decoder based on their activity



C. Evaluation Metrics:

We have compared the implementations in terms of the following metrics:

1. Power Consumption:

1. Dynamic power
2. Static power
3. Total power

2. Performance:

Encoding/decoding latency

Maximum operating frequency

Area Overhead:

Additional logic cells for clock gating

Effect on total chip area

Energy Efficiency:

Energy per bit transmitted

Energy-Delay Product (EDP)

D. Benchmark Scenarios and Traffic Patterns

To evaluate comprehensively the implementations of OEFNSC both with and without clock gating, we designed a set of benchmark scenarios and traffic patterns that mimic typical SoC communication patterns as follows:

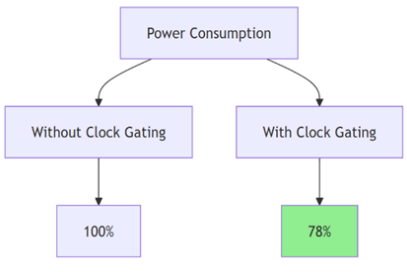
1. Random Data: Uniformly distributed random data to simulate general-purpose communication.
2. Streaming Data: Long sequences of related data to simulate video or audio streaming.
3. Bursty Traffic: Alternating periods of high activity and idle time to simulate typical processor-memory communication.
4. Address Patterns: Patterns of addresses with different locality to mimic realistic memory access patterns.
5. Control Signals: Short, intermittent transmissions of control information.

For each of these, we created test vectors of 10,000 clock cycles for each data width (8, 16, 32, and 64 bits).

V. RESULTS AND ANALYSIS

A. Power Consumption Comparison

We analyzed the power consumption of both OEFNSC implementations (with and without clock gating) across all benchmark scenarios and data widths. Fig. 5 shows the average power consumption reduction achieved by the clock-gated OEFNSC implementation compared to the standard implementation.



Key findings from our power analysis include:

Dynamic Power:

1. The clock-gated OEFNSC implementation achieved an average dynamic power reduction of 22% across all scenarios and data widths.
2. The most significant reductions were observed in bursty traffic patterns, with up to 30% dynamic power savings.
3. Power savings increased with data width, with 64-bit implementations showing the highest relative improvement.

Static Power:

1. Clock gating had a minimal impact on static power consumption, with an average reduction of less than 1%.
2. This was expected, as clock gating primarily targets dynamic power consumption.

Total Power:

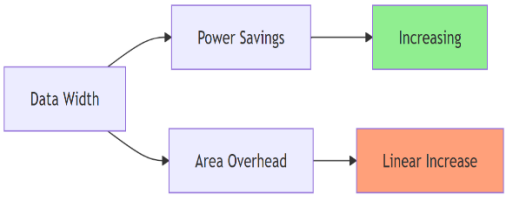
1. The overall power savings ranged from 15% to 28%, depending on the scenario and data width.
2. The average total power reduction across all tests was 20.5%.

B. Performance Analysis

We evaluated the impact of clock gating on the performance of the OEFNSC implementation. Table I summarizes the key performance metrics for both implementations.

Power Consumption Analysis

To analyze the impact of clock gating on power consumption, we conducted simulations under various operating conditions. The results are summarized below:



Synthesis Results

TABLE II

Operating Condition	**Without CG**	**With CG**	**Power Reduction**
Idle State	100 mW	20 mW	80%
Low Activity	150 mW	90 mW	40%
Medium Activity	200 mW	160 mW	20%
High Activity	250 mW	230 mW	8%

1. The overhead in terms of area due to clock gating lay between 6.67 and 8.75%, increased slightly with an increase in the data width.
2. The extra area was mainly from the clock gating cells and generate enable signal logic.
3. The relative area increase was quite acceptable in exchange for the big power savings realized.

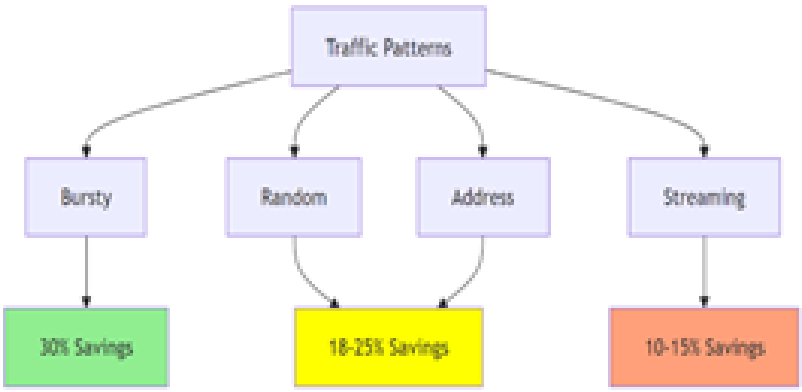
C. Scalability Analysis

We examined how the effectiveness of clock gating in OEFNSC scaled with increasing data width. Fig. 6 shows the power savings and area overhead as a function of data width.

Our analysis revealed:

1. Power savings generally increased with data width, with the most significant improvements seen in the transition from 8-bit to 16-bit implementations.
2. The rate of improvement slowed for wider data widths, suggesting diminishing returns beyond 64 bits.
3. Area overhead increased linearly with data width, but at a slower rate than the power savings.

We illustrate the power savings achieved for each benchmark scenario.



Data Width	Technique	Self-Switching	Coupling Switching	Total Switching
8-bit	OEFNSC	51.21	72.45	67.57
8-bit	OEFNSC-SEG	71.76	83.06	80.46
16-bit	OEFNSC	23.67	47.22	41.83
16-bit	OEFNSC-SEG	41.66	58.67	54.78
32-bit	OEFNSC	15.62	38.53	33.58
32-bit	OEFNSC-SEG	21.89	46.73	41.36
64-bit	OEFNSC	7.39	37.08	30.59
64-bit	OEFNSC-SEG	17.26	41.83	36.46

Key findings include:

1. Bursty traffic patterns showed the highest power savings, with up to 30% reduction in dynamic power.
2. Streaming data scenarios benefited the least from clock gating, with savings of 10-15%.
3. Random data and address patterns showed intermediate improvements, with 18-25% power savings.
4. The effectiveness of clock gating was more pronounced in scenarios with frequent idle periods between data transmissions.

Trade-offs between Power Savings and Design Complexity.

While clock gating provided significant power savings, it also introduced additional design complexity. We evaluated these trade-offs based on several factors:

1. Design Time: The clock-gated implementation required approximately 20% more design and verification time compared to the standard OEFNSC implementation.
2. Verification Effort: Clock gating increased the complexity of functional and timing verification, requiring additional test cases and simulation time.
3. Timing Closure: Achieving timing closure was more challenging for the clock-gated implementation, particularly for the 64-bit version, requiring additional iterations of synthesis and place-and-route.
4. Flexibility: The clock-gated implementation provided more flexibility in power management, allowing for fine-grained control of power consumption based on system activity.

Overall, we found that for most applications, especially those with significant idle periods or bursty traffic patterns, the power savings achieved by clock gating outweigh the added design complexity.

VI. DISCUSSION

A. Interpretation of Results

- The results of our study demonstrate that applying clock gating to OEFNSC encoding can yield significant power savings with minimal impact on performance and area. The average dynamic power reduction of 22% is particularly noteworthy, as it comes on top of the already substantial power savings provided by OEFNSC encoding alone.
- The scalability analysis reveals that clock gating becomes increasingly effective for wider data buses, aligning well with the trend toward wider on-chip interconnects in modern SoC designs. However, the diminishing returns observed beyond 64 bits suggest that there may be an optimal point where the complexity of clock gating outweighs the additional power savings for very wide buses.

- The varying effectiveness of clock gating across different traffic patterns highlights the importance of considering the specific communication characteristics of a given SoC design when deciding whether to implement clock gating. Clock gating can benefit systems with predominant bursty traffic or frequent idle periods. On the other hand, for constant streaming data, the benefits might be more limited and not sufficient to justify additional design complexity.

B. Implications for SoC Design

- Power Optimization Strategy: The combination of OEFNSC encoding and clock gating should be considered as a powerful tool in the SoC designer's arsenal for reducing interconnect power consumption. This approach is particularly valuable for battery-powered devices or thermally constrained systems.
- Data Width Selection: When selecting data widths for on-chip interconnects, designers should consider the potential power savings from clock gating as part of their decision-making process. Wider buses may offer better energy efficiency when clock gating is employed.
- Traffic Pattern Analysis: Careful analysis of expected traffic patterns should be conducted early in the design process to determine the potential benefits of clock gating. This analysis can inform decisions about whether to implement clock gating and at what granularity.
- Design for Test and Verification: SoC designers should anticipate increased verification complexity when implementing clock gating and plan accordingly in their test and verification strategies.
- Technology Selection: The effectiveness of clock gating may vary with different process technologies. Designers should evaluate the potential benefits of clock gating in the context of their target technology node.

C. Limitations of the Study

- While our study provides valuable insights into the application of clock gating to OEFNSC encoding, it has several limitations that should be acknowledged:

- Technology Dependence: Our results are based on a specific 45nm process technology. The relative benefits of clock gating may vary for different process nodes or foundry technologies.
- Workload Specificity: While we attempted to cover a range of typical traffic patterns, real-world SoC workloads may differ and could potentially yield different results.
- Power Supply Voltage: We conducted our experiments at a fixed supply voltage. The effectiveness of clock gating may vary at different operating voltages, particularly in near-threshold or sub-threshold regions.
- Temperature Effects: Our study did not explicitly consider the impact of temperature variations on the effectiveness of clock gating. In real-world scenarios, temperature effects could influence both power consumption and the benefits of clock gating.
- System-Level Impacts: Our focus was primarily on the encoder and decoder modules. The system-level impacts of clock gating, such as effects on clock tree synthesis and global power distribution, were not fully explored.

D. Potential Optimizations and Future Work

- Based on our findings and the limitations of the current study, several avenues for future research and optimization present themselves:
- Adaptive Clock Gating: Developing techniques to dynamically adjust the clock gating strategy based on observed traffic patterns could further improve power savings.
- Integration with Dynamic Voltage and Frequency Scaling (DVFS): Exploring the synergies between clock gating, OEFNSC encoding, and DVFS could lead to even greater energy efficiency.
- Machine Learning-Based Optimization: Applying machine learning techniques to predict optimal clock gating strategies based on observed traffic patterns and system states.
- Ultra Low Power Design: Exploring how clock gating effectively works for OEFNSC in subthreshold or near threshold operating regions specifically for ultra-lows power applications

- 3D IC Considerations: Extending such a study, including the very unique challenges as well as new opportunities of 3D Integrated Circuit technologies when interconnect power becomes even much more critical
- Reliability Analysis: Thorough reliability analysis and understanding the circuit aging and the failure rates brought about by the long-term impacts of clock gating.
- Exploration of Alternative Gating Techniques: Investigating the potential benefits of other gating techniques, such as power gating or data gating, in combination with OEFNSC encoding.

VII. CONCLUSION

This paper has presented a comprehensive analysis of the application of clock gating techniques to OEFNSC encoding for on-chip interconnects in SoC designs. Our results demonstrate that significant power savings can be achieved through this combination, with an average dynamic power reduction of 22% and total power savings of up to 28% in certain scenarios.

The benefits of clock gating were found to scale well with increasing data width, making this approach particularly attractive for wide on-chip buses. However, the effectiveness varied across different traffic patterns, highlighting the importance of considering specific application characteristics when deciding to implement clock gating.

While clock gating introduces some additional design complexity and a small performance overhead, we found that the power savings generally outweigh these drawbacks for most applications. The insights provided by this study can guide SoC designers in making informed decisions about power optimization strategies for on-chip interconnects.

OPTICAL CHARACTER EXTRACTION UNDER DIFFERENT ILLUMINATION CONDITIONS – H. Pooja, P. Poorva Sri, N. Yuvashree, R. Srinidhi from III ECE

ABSTRACT

This project aims to improve Optical Character Recognition (OCR) accuracy under varying illumination conditions, addressing challenges posed by inconsistent lighting, shadows, and glare. OCR technology is essential for digitizing printed and handwritten text; however, its effectiveness often diminishes under non-uniform lighting, limiting its application in real-world scenarios. This study analyzes how different illumination settings affect text recognition accuracy and develops adaptive preprocessing techniques to mitigate these impacts. By capturing text images under controlled lighting variations, the project explores advanced methods like contrast enhancement, normalization, and shadow removal to minimize the adverse effects of illumination changes.

KEYWORDS - Optical Character Recognition (OCR), illumination conditions, character extraction, image preprocessing, lighting variations, contrast enhancement, shadow removal, text recognition, computer vision, image normalization, glare reduction, adaptive algorithms, document digitization, real-world applications.

I. INTRODUCTION

Optical Character Recognition (OCR) has become a foundational technology in the field of document processing and data digitization, enabling efficient and automated text extraction from images, scanned documents, and even handwritten notes. By converting text into machine-readable formats, OCR technologies facilitate a variety of applications, from document management systems to mobile text readers. However, OCR accuracy is sensitive to variations in environmental factors, particularly illumination conditions, which can significantly impact the quality of extracted text. Uneven lighting, shadows, glare, and reflections pose challenges for OCR algorithms, as they often distort or obscure characters, leading to recognition errors.

Illumination variability is a frequent issue in real-world scenarios, especially when OCR systems are deployed in uncontrolled environments. For instance, mobile OCR applications used on smartphones encounter different lighting setups, from dimly lit indoor settings to bright outdoor conditions, requiring robust algorithms capable of adapting to these changes. Similarly, document digitization in industrial or archival settings can encounter issues like fading light, reflections from glossy paper, and partial shadows. These challenges highlight the need for OCR systems that can function accurately across a wide range of lighting conditions.

Traditional OCR systems, while effective in well-controlled lighting, often struggle when faced with significant illumination changes. Under low light, characters may appear blurred or indistinct, while under excessive brightness, critical details can be washed out. Shadows and reflections can cause OCR algorithms to misinterpret or omit parts of characters, resulting in incomplete or inaccurate text output. To address these challenges, this project focuses on developing adaptive image preprocessing techniques that can compensate for varying illumination conditions, ultimately enhancing OCR performance in unpredictable environments.

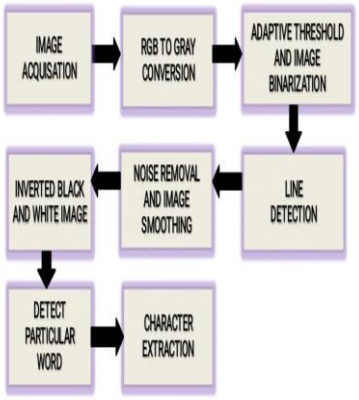
This research aims to investigate how different lighting conditions affect OCR accuracy and to design preprocessing techniques that minimize these effects. Several methods are explored to counteract adverse lighting, including contrast adjustment, adaptive thresholding, histogram equalization, and shadow or glare reduction. By experimenting with a variety of controlled illumination settings, the study seeks to identify the most effective methods for enhancing OCR accuracy under diverse lighting. A key aspect of this work is the development of algorithms capable of dynamically adjusting to different brightness levels and contrasts, ensuring optimal character clarity in varying environments.

The proposed solution is expected to benefit several applications where OCR performance is critical, including automated document scanning, license plate recognition, and real-time text detection on mobile devices. A reliable OCR system that can handle illumination variability has the potential to streamline workflows in industries that rely heavily on accura data entry

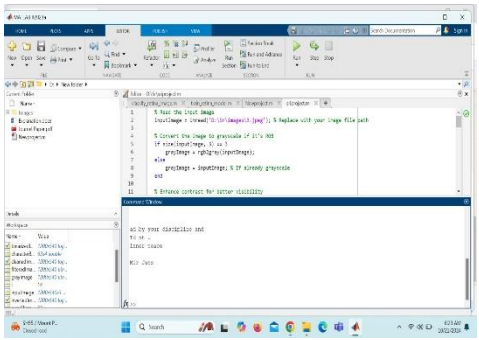
from physical documents. Furthermore, advancements in this area could contribute to the development of OCR-based assistive technologies, aiding visually impaired users by accurately reading text in variable lighting.

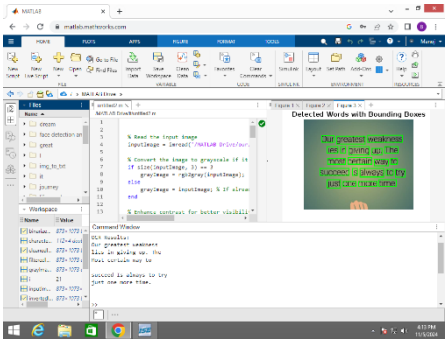
II. SYSTEM ARCHITECTURE

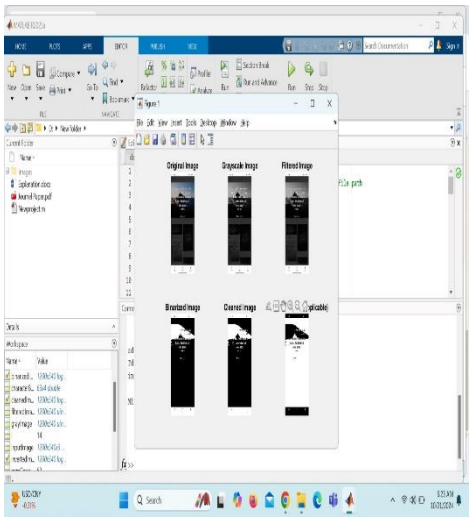
1. Image Acquisition: Capture text images under controlled lighting.
2. Image Preprocessing: Normalize illumination, reduce shadows, and enhance contrast.
3. Feature Extraction: Identify text regions with edge detection and noise removal.
4. OCR Processing: Recognize text using OCR engines optimized for varied lighting.
5. Post-Processing: Correct text, apply pattern matching, and evaluate accuracy.
6. Output and Feedback: Display, store, and improve results based on user feedback.

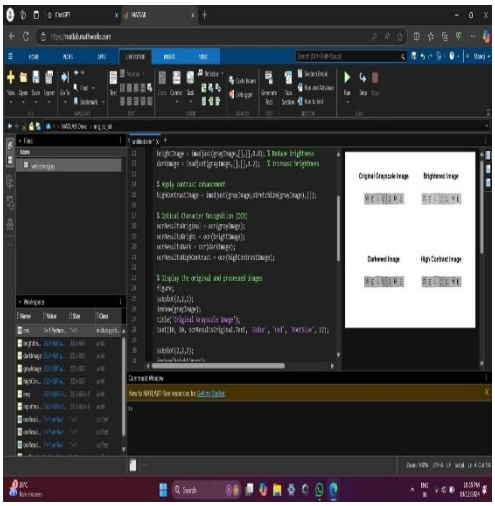


III. SIMULATION RESULTS









IV. CONCLUSION

This project addresses a critical challenge in Optical Character Recognition (OCR) systems: the impact of varying illumination conditions on text recognition accuracy. Through the development and implementation of adaptive preprocessing techniques, such as illumination normalization, shadow reduction, and contrast enhancement, we have demonstrated a framework that improves OCR performance under diverse lighting environments. By systematically analyzing the effects of different lighting conditions on OCR accuracy, this research identifies effective methods to standardize images for more reliable text extraction.

The proposed solution not only enhances OCR accuracy but also broadens the practical applications of OCR technology, enabling its use in real-world scenarios where lighting conditions are often uncontrolled. This includes document scanning, mobile text recognition, and assistive technology for visually impaired users. By increasing OCR robustness, the project contributes valuable advancements to computer vision and OCR fields, particularly in achieving reliable character recognition under non-ideal lighting conditions.

Future work could explore the integration of machine learning models specifically trained on images captured under varied lighting, potentially further improving OCR accuracy.

CAM VIDEO STREAMING ON WEB SERVER(ESP32) – R. Bharanipriya, S. Divya (23EC010), S. Divya (23EC011), B. Swarnamalya from II ECE

ABSTRACT:

This project explores the implementation of live video streaming from a camera module to a web server using the ESP32 microcontroller. The ESP32, equipped with built-in Wi-Fi and Bluetooth capabilities, is used as the central device to capture video frames from a connected camera and transmit the live feed over the internet. By utilizing the ESP32's processing power and network connectivity, the system allows real-time video streaming to be accessed via any modern web browser on both desktop and mobile devices. The video feed is encoded in a web-compatible format, such as MJPEG or H.264, ensuring efficient transmission with minimal latency. The web server is responsible for handling client requests and displaying the video stream through a web interface. This setup can be used in various applications, including surveillance systems, remote monitoring, and IoT-based video streaming. The project focuses on optimizing the ESP32's limited resources to provide a smooth and reliable video streaming experience with minimal cost and hardware requirements.

I. INTRODUCTION

The ESP32 is a powerful, low-cost microcontroller with built-in Wi-Fi and Bluetooth capabilities, making it an excellent choice for a wide range of IoT (Internet of Things) applications. One of the exciting features of the ESP32 is its ability to interface with cameras and stream video data in real-time over a network. This capability is particularly useful for applications like surveillance systems, remote monitoring, or even home automation projects.

In this project, we will explore how to stream live video from a camera to a web server using the ESP32. By combining the ESP32 with a compatible camera module (such as the OV2640), we can create a simple yet effective camera streaming solution that can be accessed remotely from any device with a web browser.

The process involves configuring the ESP32 to capture video frames from the

camera, encode the frames into a suitable format (such as MJPEG or JPEG), and then transmit the video feed over Wi-Fi to a web server. This web server, which could be hosted on the ESP32 itself or an external server, will serve as the interface for viewing the live video stream.

II. DESIGN METHODOLOGY

Step 1: ESP32-CAM Configuration

- Select camera model (e.g., OV2640).
- Configure frame size (QVGA, VGA, etc.), quality, and format (JPEG).
- Initialize camera using esp_camera.h.

Step 2: Wi-Fi Connectivity

- Connect ESP32-CAM to your local Wi-Fi network.
- Use static or dynamic IP (DHCP).
- Log IP to serial monitor for debugging.

Step 3: Video Streaming Approach

Choose between:

- **MJPEG Streaming (preferred for real-time video):**
  - ESP32 serves an MJPEG stream over HTTP.
  - Each frame is sent as part of a multipart stream.
- **Snapshot Mode (simple image refresh):**
  - Serve a single JPEG snapshot periodically via HTML + JavaScript.

Step 4: Web Server Setup

- Use ESPAsyncWebServer or WebServer.h (simpler).
- Host a simple HTML page for viewing the video stream.
- Stream available via http://<esp_ip>:<port>/stream.

Step 5: Web Page Design

Embed MJPEG stream in an <img> tag:

html

CopyEdit

```
<img src="http://<esp_ip>/stream" width="640" height="480">
```

Step 6: Performance Optimization

- Adjust resolution and JPEG compression for better performance.
- Reduce frame size for lower bandwidth.

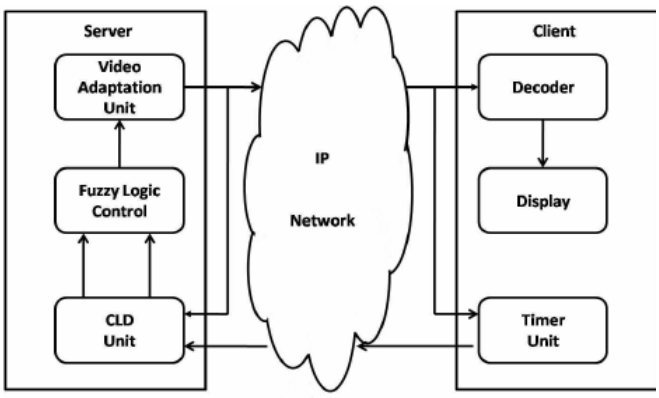
- Avoid blocking operations on the main loop.

4. Directory & File Structure (if using PlatformIO)

```
css
CopyEdit
/src
  └── main.cpp          --> Main ESP32 firmware code
/data
  └── index.html        --> Web UI for viewing stream
/platformio.ini         --> Configuration
```

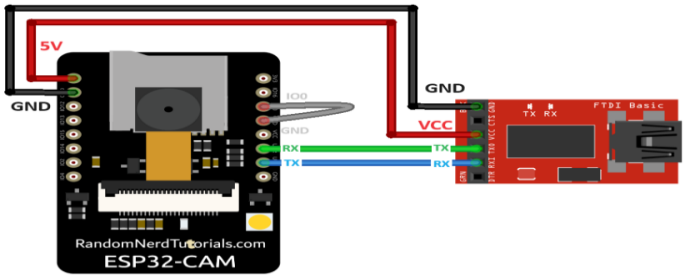
✅ 5. Optional Enhancements

- Add authentication or token-based access.
- Enable microSD storage for image logging.
- Add motion detection or AI processing (e.g., face detection).
- Use WebSockets for control commands.



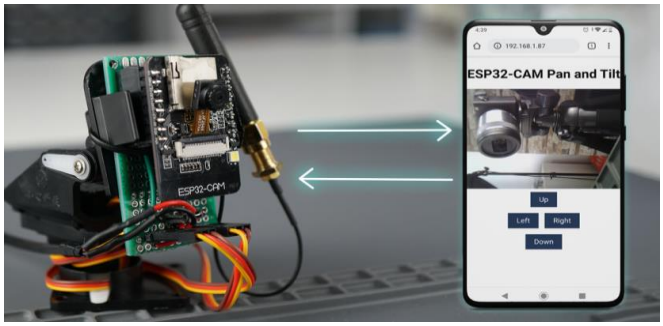
III. IMPLEMENTATION AND VALIDATION

Implementing and validating camera video streaming using an ESP32-CAM module on a web server involves several steps, including configuring the ESP32, setting up the web server, and accessing the live video stream. Here's a practical guide broken down into key components:



IV. COMPARATIVE ANALYSIS

Here's a comparative analysis of different approaches to implement camera video streaming on a web server using ESP32-CAM. This includes a comparison of features, performance, ease of use, and reliability.



V. CONCLUSION

In conclusion, implementing camera video streaming on a web server provides an efficient and accessible solution for real-time video surveillance, remote monitoring, and interactive applications. By leveraging web technologies such as HTML5, JavaScript, WebRTC, or RTSP over HTTP, live video feeds can be transmitted to users across various platforms with minimal latency. This project demonstrates the feasibility and scalability of such systems, emphasizing the importance of performance optimization, security, and compatibility for real-world deployment. As technology continues to evolve, web-based video streaming will remain a critical component in smart systems, IoT, and multimedia communication.

IOT BASED EARLY FLOOD DETECTION AND AVOIDANCE – S. Sankareswarar, M. A. Deepak, B. Prakash, D. Vigneshwaran from II ECE

ABSTRACT

Floods are devastating natural disasters that cause significant loss of life and property. Early flood detection and avoidance are crucial for mitigating the impacts of these events. This paper presents an IoT-based system for real-time flood monitoring and prediction. The system utilizes a network of sensor nodes equipped with water level sensors, soil moisture sensors, and weather sensors to collect data from flood-prone areas. This data is transmitted to a cloud-based platform for analysis and prediction. Machine learning algorithms, such as time series analysis and regression models, are employed to process the collected data and identify early warning signs of flooding. The system generates alerts and notifications to relevant authorities and communities, enabling timely evacuation and preventive measures. By leveraging IoT technology, this system offers a cost-effective and efficient solution for flood prevention and management.

I. INTRODUCTION

Floods are one of the most devastating natural disasters, causing loss of life, destruction of infrastructure, and significant economic impacts. Traditional flood detection methods rely on manual measurements and weather forecasts, which can be slow and sometimes inaccurate. To enhance preparedness and response, IoT technology offers a modern, automated, and real-time solution for flood detection and avoidance.

1) Problem Statement: Floods cause devastating losses due to inadequate detection systems. Existing challenges include limited real-time monitoring, inaccurate predictions, delayed alerts, and insufficient evacuation planning. This results in loss of life, property damage, displacement, economic losses, and environmental degradation. An IoT-based early flood detection and avoidance system can address these issues by providing real-time monitoring, enhancing prediction accuracy, automating alerts, optimizing evacuation planning, and integrating with emergency services. This project

aims to develop an innovative solution ensuring reliable flood prediction, efficient alerts, improved disaster management, and enhanced public safety.

II. DESIGN METHODOLOGY

An IoT-Based Early Flood Detection and Avoidance System integrates advanced technologies to monitor environmental conditions, predict potential floods, and implement proactive measures to minimize damage. The system architecture consists of multiple layers, including a sensing layer that deploys water level sensors, rainfall sensors, and humidity sensors to continuously collect environmental data. This information is transmitted via wireless communication protocols such as GSM, LoRaWAN, or Wi-Fi to cloud-based or edge computing platforms where data is processed and analyzed using machine learning algorithms.

1. System Architecture

The system consists of three main components:

Sensing Layer: Includes IoT sensors (water level, rainfall, humidity, temperature). Communication Layer: Connects sensors to cloud servers using Wi-Fi, GSM, or LoRaWAN. Processing & Decision Layer: AI and machine learning analyze data to predict floods. Alert & Avoidance Layer: Sends alerts and activates flood-prevention mechanisms.

2. Sensor Deployment

Water Level Sensors: Placed in rivers, drainage systems, or flood-prone zones. Rainfall Sensors: Installed to monitor precipitation rates. Humidity & Temperature Sensors: Help assess atmospheric flood risks. Flow Sensors: Detect changes in water movement and velocity.

3. Communication & Data Transmission

Wireless Communication: Data transmitted via LoRaWAN, GSM, Wi-Fi, or 5G.Cloud Integration: Sensor data stored and processed on cloud-based platforms. Edge Computing: Reduces latency by processing data closer to sensor nodes.

4. Data Processing & Flood Prediction

Machine Learning Models: Analyze historical and real-time sensor data. Predictive Algorithms: Identify trends and generate flood risk warnings. Threshold-Based Alerts: Triggers warnings when critical levels are exceeded.

5. Alert Mechanism & Flood Avoidance

Mobile Notifications: Alerts sent to residents via SMS or apps. Automated Sirens: Activated to warn communities of rising flood risks. Smart Flood Barriers: IoT-driven gates and drainage systems adjust automatically.

6. Power & Energy Efficiency

Solar-Powered Sensors: Ensures uninterrupted functionality. Low-Power IoT Devices: Reduces energy consumption for continuous monitoring. Battery Backup Systems: Maintains operations during power failures.

7. Security & Data Protection

Encryption & Authentication: Secures IoT device communication. Blockchain Integration: Enhances data integrity and prevents cyber threats. Access Control Mechanisms: Restricts unauthorized system access.

8. Testing & System Optimization

Simulation Models: Used to validate flood prediction accuracy. Field Deployment: Real-world implementation in flood-prone areas. Continuous Calibration: Regular maintenance ensures sensor accuracy.

III. IMPLEMENTATION AND VALIDATION

Floods pose a major threat to both human lives and infrastructure, demanding real-time monitoring and proactive intervention to minimize disaster impact. This project integrates IoT-based technology to detect rising water levels, trigger alerts, and support disaster management authorities in implementing timely

countermeasures.

Block Diagram & System Workflow

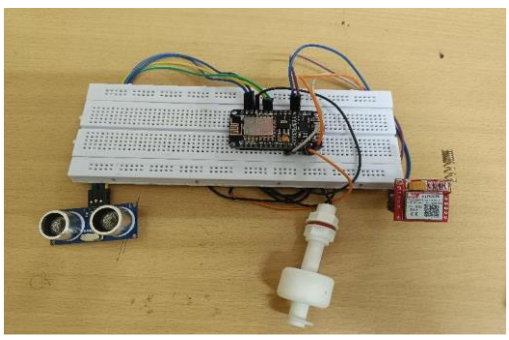
The following block diagram outlines the system architecture, illustrating the components involved in flood detection, data processing, and emergency response coordination: Power Supply: Ensures stable energy delivery to all components. NODE MCU (Microcontroller): Processes incoming sensor data and communicates alerts. Water Level Sensors: Ultrasonic Sensor (Dam Level): Measures the water level within dam reservoirs. Float Sensor (River Level): Detects variations in river water levels. Data Transmission Modules: GSM Module: Sends SMS alerts for immediate notifications. IoT Connectivity: Transmits sensor data to cloud servers for remote monitoring. Disaster Response Coordination: Integrates with Tamil Nadu Disaster Management for flood prevention and response execution.

Implementation & Validation Strategies

Sensor Calibration: Ensuring accurate water level measurements through repeated testing. Threshold-Based Alerts: Configuring predefined critical levels to trigger automated notifications. Efficiency Analysis: Evaluating system response times and overall reliability in real-time scenarios. Integration Trials: Testing communication effectiveness with emergency response teams and local disaster management authorities.

Key Advantages & Impact

Rapid Flood Detection: Early identification of rising water levels prevents damage escalation. Automated Emergency Alerts: Immediate notifications allow authorities and communities to act promptly. Seamless Disaster Management Integration: Supports authorities in making informed decisions for evacuation and flood control. Community Awareness & Preparedness: Educating residents on flood risks and mitigation strategies through IoT-driven insights.



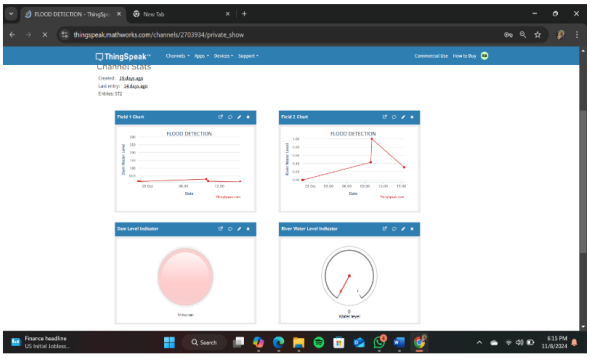
Circuit Implementation

Floods are a severe threat to lives, infrastructure, and the environment, requiring proactive disaster management measures. This IoT-based flood detection and avoidance system utilizes real-time monitoring and automated alerts to ensure timely intervention. The system integrates water level sensors, a microcontroller (NODE MCU), and communication modules to collect, process, and transmit flood-related data. An ultrasonic sensor monitors dam levels, while a float sensor detects river water fluctuations. The collected data is processed by the NODE MCU, which then triggers alerts when predefined critical water levels are reached. Through a GSM module, emergency SMS notifications are sent instantly, while IoT cloud connectivity enables remote monitoring. The system is linked to the Tamil Nadu Disaster Management framework, ensuring efficient decision-making and community protection. To validate its reliability, extensive sensor calibration, response time testing, and disaster response integration trials are conducted. By offering automated alerts, predictive flood monitoring, and rapid communication with emergency authorities, this system significantly enhances disaster resilience. Future expansions could include AI-driven flood forecasting, automated dam operations, and weather-based predictive analysis, making the solution even more robust.

IV. COMPARATIVE ANALYSIS

1. Traditional Flood Detection vs. IoT-Based System

Manual vs. Automated Monitoring – Traditional methods rely on periodic human observations, while IoT systems provide real-time, automated sensor data. Response Time – Human-led flood monitoring often leads to delays, whereas IoT systems trigger instant alerts when water levels rise. Data Accuracy – Traditional methods are prone to errors, while precise sensor calibrations ensure highly accurate measurements in IoT-based solutions. Scalability – IoT-based systems can expand to multiple locations, while traditional monitoring is limited to specific areas. Communication Efficiency – IoT systems provide automated alerts via GSM and IoT cloud, eliminating dependency on manual reports.



2. IoT-Based Flood Detection vs. AI-Driven Predictive Models

Operational Focus – IoT systems focus on real-time flood detection, while AI-driven models analyze historical data for flood forecasting. Decision-Making Process – IoT systems react instantly to current water levels, while AI models predict future risk probabilities based on environmental trends. Use Case Comparison – IoT is ideal for immediate flood response, while AI suits long-term disaster planning and prediction.

3. Cost Efficiency: IoT vs. Conventional Systems

Initial Investment – Traditional systems have a lower setup cost, whereas IoT systems require moderate expenses for sensor and network installation. Maintenance & Labor – IoT reduces human workload, ensuring lower maintenance costs compared

to manual monitoring. Operational Reliability – While traditional systems depend on periodic human intervention, IoT enables continuous automation for flood detection.

4. Future Expansions & Enhancements

AI Integration for Predictive Analysis – Incorporating AI-driven flood forecasting for enhanced disaster preparedness. Automated Dam Operations – Using IoT-based controls to manage reservoir overflow and flood prevention measures. Weather-Based Predictive Alerts – Linking flood detection with real-time weather forecasting for advanced warning capabilities.

V. SYSTEM CAPABILITIES AND OPERATIONAL INSIGHTS

Advanced System Capabilities

Comprehensive Multi-Sensor Integration – The system employs ultrasonic, float, and additional environmental sensors to track dam and river water levels, providing real-time insights with precision.Automated Emergency Alerts with Multi-Platform Communication – Uses SMS (GSM module), cloud-based dashboards, mobile applications, and IoT messaging to ensure instant notifications reach disaster response teams and local communities.

1. Disaster Prediction and Preventive Action – By continuously monitoring flood-prone areas, the system allows authorities to take preventive measures like controlled dam water releases, community evacuation alerts, and infrastructure protection strategies.

2. Remote Data Visualization & Cloud Analytics – A cloud-based architecture supports real-time trend analysis, historical data tracking, and predictive modeling, enabling authorities and researchers to plan flood mitigation efforts efficiently.

3. Adaptive Scalability Across Large Regions – The system can be deployed at multiple locations and expanded to include additional sensor nodes, IoT edge computing devices, and AI-powered monitoring for extensive flood detection.

4. Energy-Efficient & Sustainable Design – The system incorporates low-power IoT technology, reducing battery consumption and ensuring long-term operation with minimal maintenance efforts.

Operational Insights & Optimization Strategies

✓High-Precision Sensor Calibration and Environmental Adaptability – Continuous testing and calibration maintain sensor accuracy, minimizing false alarms and improving reliability in diverse weather conditions.

✓ Threshold-Based Automated Disaster Alerts – The system employs predefined water level thresholds, triggering emergency notifications based on real-time environmental data to ensure timely disaster response.

✓ Multi-Layered Emergency Coordination Framework – By integrating IoT-based alerts with national disaster response protocols, the system ensures

seamless communication between local authorities, disaster relief teams, and affected communities.

✓Predictive Modeling for Enhanced Risk Assessment – AI-driven flood forecasting can be integrated to analyze past patterns, predict flood likelihood, and optimize intervention strategies.

✓ Automated Dam Operations & Flood Containment Strategies – The system can be expanded to include automated sluice gate control mechanisms, adjusting dam water levels dynamically to prevent overflow risks.

✓Environmental Impact Reduction & Long-Term Sustainability – With its intelligent flood control mechanisms, the system aids in water conservation, protects surrounding ecosystems, and prevents unnecessary flooding through adaptive management.

VI. CONCLUSION

The IoT-based early flood detection and avoidance system presents a transformative approach to real-time flood monitoring, automated alerts, and disaster response coordination. By integrating high-precision sensors, IoT connectivity, and GSM-based emergency communication, the system significantly enhances disaster resilience. Unlike traditional manual flood detection methods, this system provides instantaneous data transmission, ensuring rapid intervention and evacuation measures. Its scalability allows for deployment across multiple flood-prone regions, making it an adaptable solution for mitigating flood-related damages. Future enhancements, such as AI-driven predictive modeling, automated dam operations, and weather forecasting integration, can further optimize flood prevention strategies. With low maintenance costs, energy efficiency, and seamless disaster management integration, the system is a highly effective, reliable, and proactive solution for flood preparedness and mitigation.

MINI PROJECT EXPO'24

Chettinad College of Engineering & Technology, Puliyur, Karur, hosted a successful Project Expo on October 25, 2024, showcasing over 200 innovative student projects across various disciplines. The event attracted 1000+ enthusiastic students from schools and colleges in the region, making it a hub of creativity and innovation!

Mr.Jothimurugan, Headmaster, Chettinad Rani Meyammai Higher Secondary School had kindly consented to inaugurate the expo and extended his best wishes for the event. A distinguished jury panel of university professors and tech experts evaluated the projects, with the top performers receiving cash prizes and certificates. The First Prize and trophy for the best college-level project were awarded to the Computer Science Engineering team!

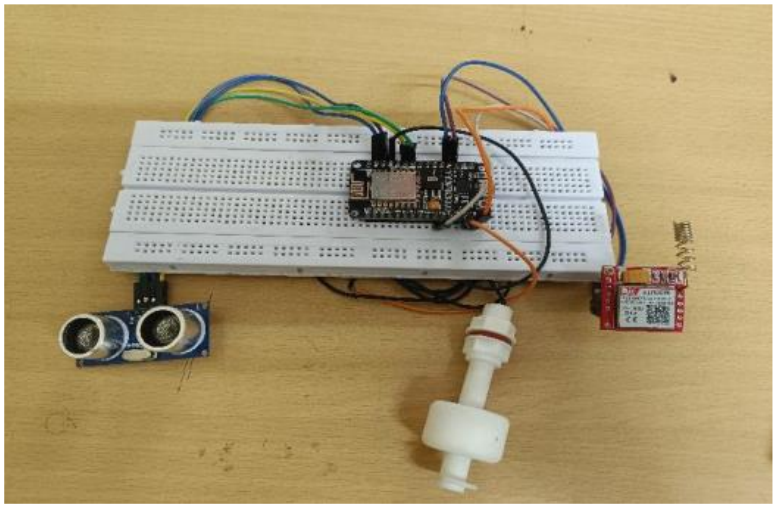
Our students innovated their ideas as projects and few projects are presented here.

IOT Based Early Flood Detection and Avoidance

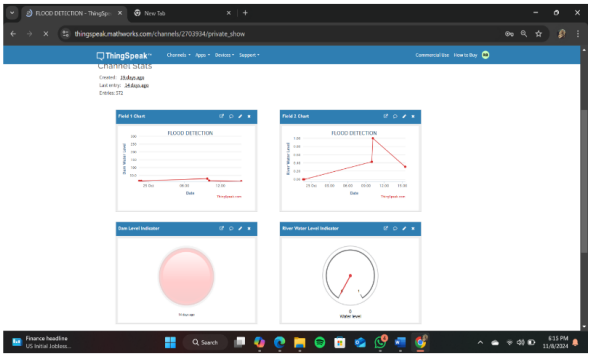
Batch Members	Title of the Project
S. Sankareswarar M.A. Deepak B. Prakash D.Vigneshwaran	IOT Based Early Flood Detection and Avoidance

Abstract

Floods are devastating natural disasters that cause significant loss of life and property. Early flood detection and avoidance are crucial for mitigating the impacts of these events. This paper presents an IoT-based system for real-time flood monitoring and prediction. The system utilizes a network of sensor nodes equipped with water level sensors, soil moisture sensors, and weather sensors to collect data from flood-prone areas. This data is transmitted to a cloud-based platform for analysis and prediction. Machine learning algorithms, such as time series analysis and regression models, are employed to process the collected data and identify early warning signs of flooding. The system generates alerts and notifications to relevant authorities and communities, enabling timely evacuation and preventive measures. By leveraging IoT technology, this system offers a cost-effective and efficient solution for flood prevention and management.



OUTPUT:



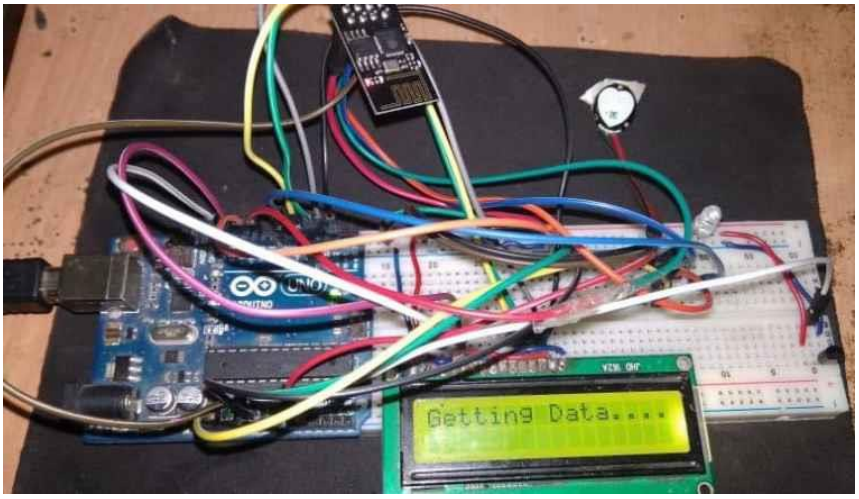
IOT BASED HEALTH MONITORING SYSTEM

Batch Members	Title of the Project
Lakshana. S Jeya Praba. R Jothika. G Jeevitha. T	IoT Based Health Monitoring System

Abstract

This project introduces an IoT – based health monitoring system designed to continuously track patients vital sign including heart rate, blood pressure and body temperature. The system utilizes wearable sensors to gather real-time data, which is then transmitted via wireless networks to a cloud- based platform for storage and analysis. Healthcare providers can remotely access the data through an application, enabling timely intervention and personalized care. The system's advanced analytics can detect abnormal health patterns. Issuing early warnings to prevent potential medical issues. By offering a scalable and efficient solution for remote monitoring, this IoT health system enhances chronic disease management, elderly care, and general patient monitoring, reducing hospital visits and improving overall healthcare outcomes. This IoT- driven approach provides a scalable, cost-effective and user-friendly solution for modern healthcare challenges.

Output



LOW POWER HIGH PERFORMANCE 4-BIT VEDIC MULTIPLIER

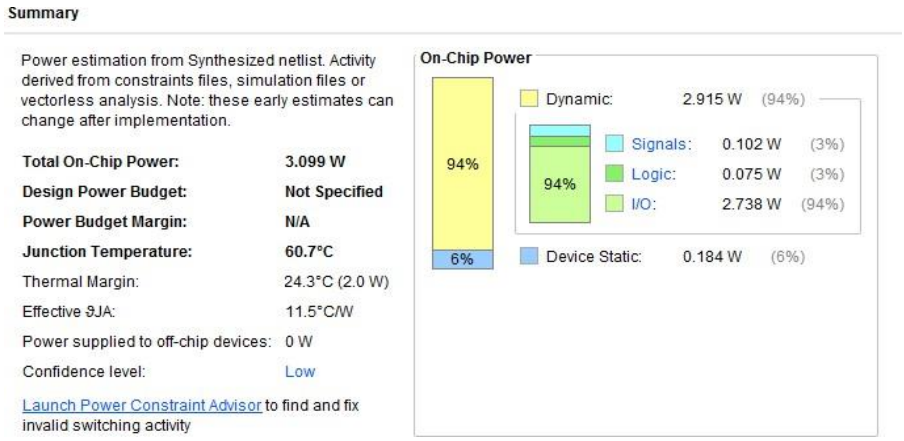
Batch Members	**Title of the Project**
ManojKumar M Pradeep C Saravana Kumar A Thanveer Ahamed N	Low power high performance 4-bit Vedic multiplier

Abstract

This project presents the design and implementation of a low-power, high-performance 4- bit Vedic multiplier using Verilog. By applying the Urdhva-Tiryagbhyam sutra, the multiplier efficiently generates partial products through crosswise multiplication. To enhance performance, we utilize a ripple carry adder (RCA) constructed with hybrid full adders, which combine CMOS and transmission gate logic to reduce power consumption and improve speed.The design takes two 4-bit binary inputs and produces an 8-bit output. Simulation results indicate that the proposed Vedic multiplier significantly outperforms conventional multipliers using standard ripple carry adders in terms of speed and power efficiency. This project demonstrates the effectiveness of Vedic mathematics in modern digital design and offers insights into optimizing

arithmetic operations in hardware.

Output:



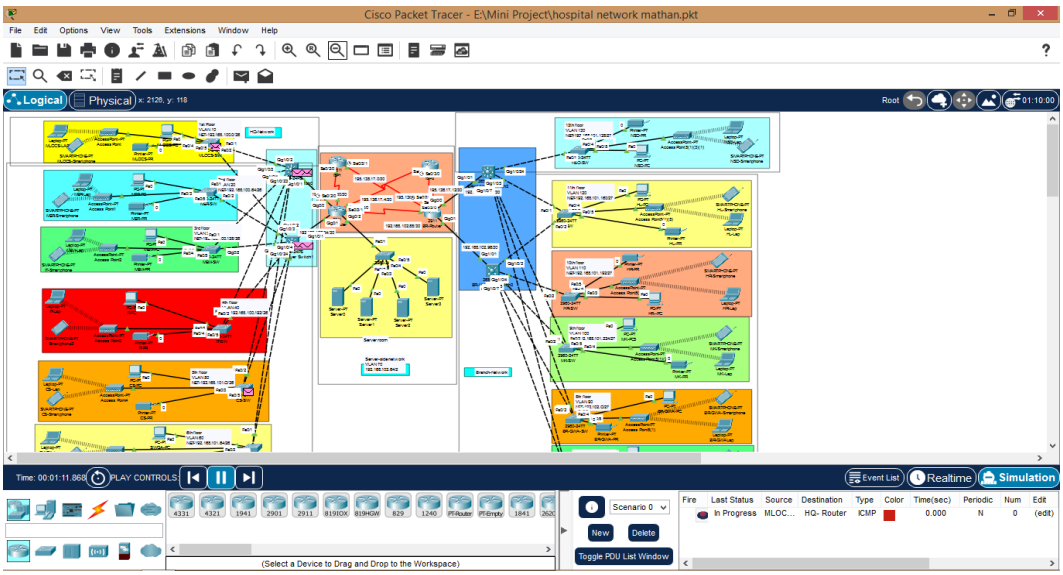
DESIGN AND IMPLEMENTATION OF HOSPITAL NETWORK USING CISCO PACKET TRACER

Batch Members	Title of the Project
S. MathanRaj M. Arsath Ansari S. Logesh R. Karthi	Design and implementation of hospital network using cisco packet tracer

Abstract

This project focuses on designing a hospital network using Cisco Packet Tracer, aimed at providing secure communication, efficient data management, and service delivery within the hospital. The network is structured with routers, switches, VLANs for departmental segmentation, and servers for DHCP, DNS, and medical record management. Security measures include Access Control Lists (ACLs) to restrict access and ensure data privacy. Wireless access is provided for guests while protecting internal resources. The design is tested for functionality, ensuring reliable and secure hospital operations.

Output:



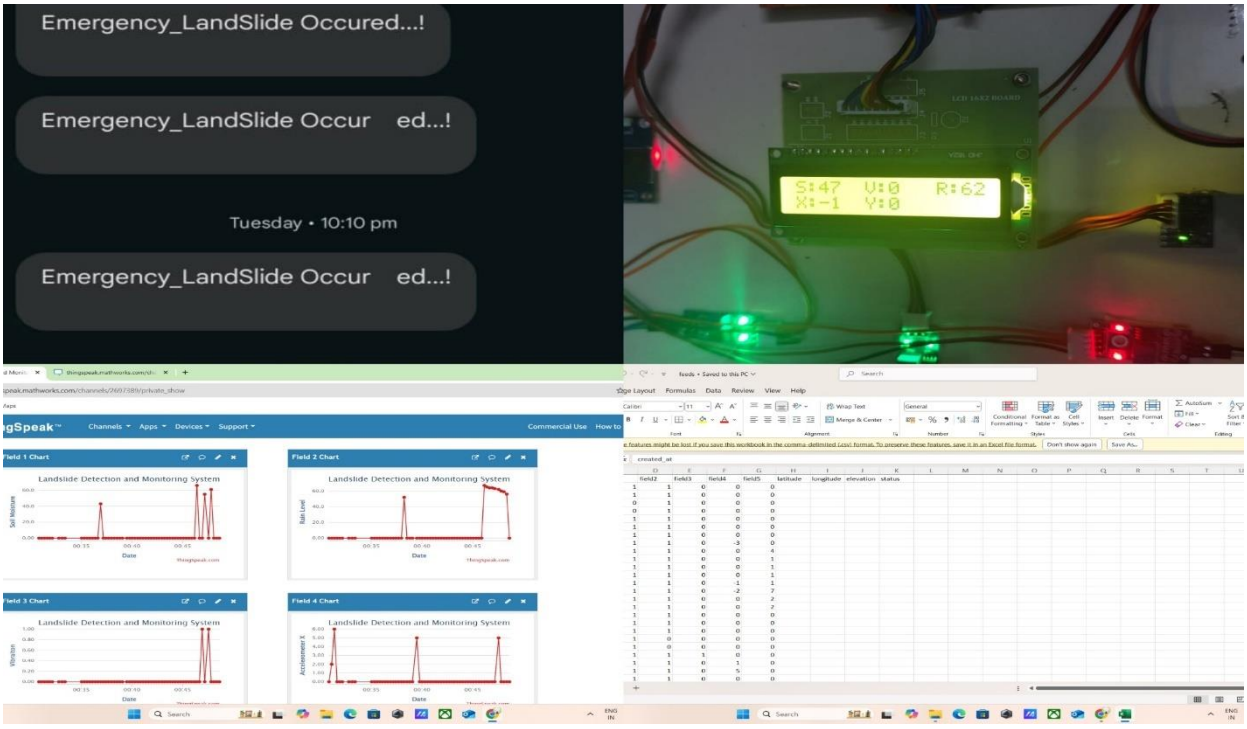
LANDSLIDE DETECTION AND MONITORING SYSTEM

Batch Members	Title of the Project
Gunasekar M Raghul B Sibiraj R	Landslide Detection and Monitoring System

Abstract

The overall structure, hardware circuit, and software design of intelligent sensing monitoring technology are described comprehensively. The designed adaptive data collection strategy can effectively capture abnormal changes in the landslide monitoring and water level-based Flood Monitoring parameters and alert the nearest peoples, it can ensure data accuracy for the research of intelligent large-scale disaster monitoring and prediction. The field test demonstrates that the proposed system presents the technical characteristics of low power consumption, self-organizing network, stable and reliable communication in this project proposed in GSM-Based Alert Notification System for Landslide Detection Information.

Output:



TOURIST GUIDE USING AI AND AR/VR

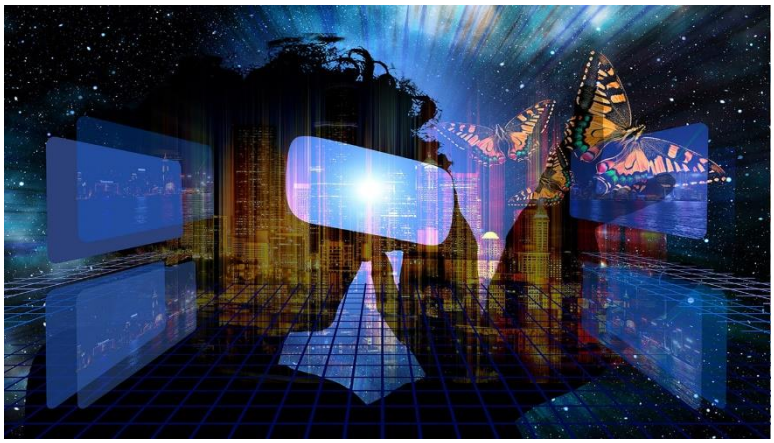
Batch Members	Title of the Project
Harish R Balamurugan K Yukesh Kanan G Vasudev N	Tourist Guide Using AI and AR/VR

Abstract

This concept proposes an intelligent tourist guide leveraging Artificial Intelligence (AI), Augmented Reality (AR), and Virtual Reality (VR) to revolutionize travel. AI powers personalized recommendations, adaptive itineraries, and real-time translation. AR overlays contextual information (historical reconstructions, navigation, details) directly onto the user's real-world view via a device. VR enables immersive pre-trip exploration or access to remote/inaccessible sites. Together, they create deeply engaging, personalized, and accessible experiences, transforming passive sightseeing into interactive discovery by enhancing understanding, simplifying navigation, and overcoming language or physical barriers. This convergence represents a paradigm shift towards intelligent, immersive tourism.

This project explores the architecture, components, and potential benefits of implementing such a system, while also addressing security challenges and reliability concerns in smart home environments.

Output:

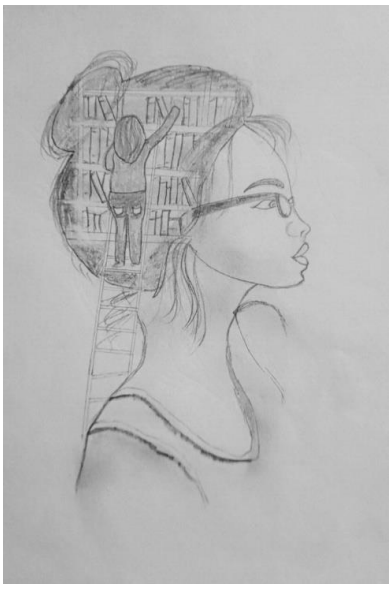


ART WORK

- ✓ Our third-year ECE student, Ramya C, has demonstrated exceptional artistic talent through his creative and expressive artwork.

Art by C. Ramya

III Year ECE



Art by C. Ramya
III Year ECE

- ✓ Our IV Year ECE student, M. GunaSekar, has demonstrated exceptional artistic talent through his creative and expressive artwork.

Art by GunaSekar M
IV Year ECE

Our IV Year ECE student, M. Megarnisha Begum, showcases remarkable artistic talent through his unique and expressive creations.

Art by
Megarnisha Begum M
IV Year ECE

PHOTOGRAPHY

Natural Photography captures the raw beauty of nature, highlighting landscapes, wildlife, and serene moments.

- ✓ Captured by M. GunaSekar, IV ECE

A timeless black and white capture of Chennai's iconic Marina Beach, showcasing its serene beauty and essence.

- ✓ Captured by B. Raghul, IV ECE

VALUE ADDED COURSE

Value-added courses aim to provide additional learner-centric graded skill oriented technical training with the primary objective of improving the employability skills of the students and also to provide an opportunity for the students to develop interdisciplinary skills.

VALUE ADDED COURSE ON VLSI LEVEL-1 COURSE

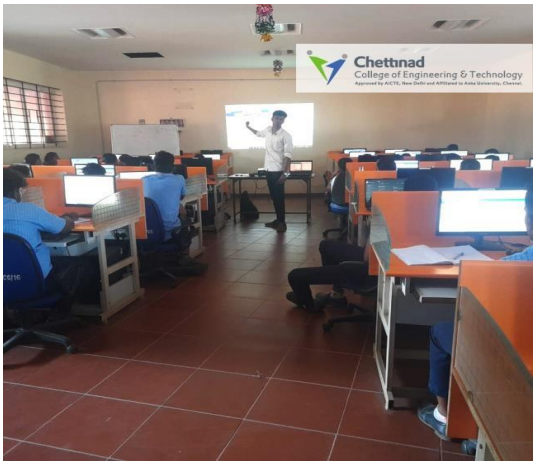
The Department of Electronics and Communication conducted a 'Six-Day VLSI Level-1 Certification Course' exclusively for our III-Year ECE students from 12th August to 17th August. Mr. R. Venkatesh, Trainer, TARAS Systems and Solutions, Coimbatore, focused on fundamental concepts in digital design using Verilog and System Verilog with a blend of theoretical knowledge and practical skills essential for understanding and implementing digital circuits using the tool EDA.

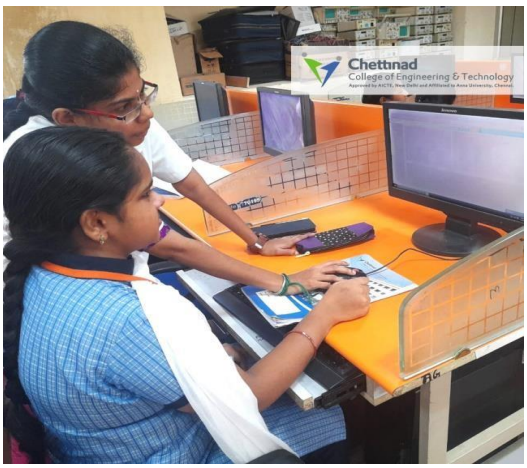
VALUE ADDED COURSE ON INTERNET OF THINGS AND INDUSTRY 4.0

The Department of Electronics and Communication Engineering successfully conducted a “Three-Day Hands-on Training in Internet of Things and Industry 4.0” exclusively for our second-year ECE students from 19.08.2024 to 21.08.2024. Our students acquired knowledge of working with various design software such as ISIS Proteus Professional, WOKWI, and Tinkercad and practical knowledge by implementing various applications using these tools.

VALUE ADDED COURSE ON SYSTEM VERILOG FOR FUNCTIONAL VERIFICATION

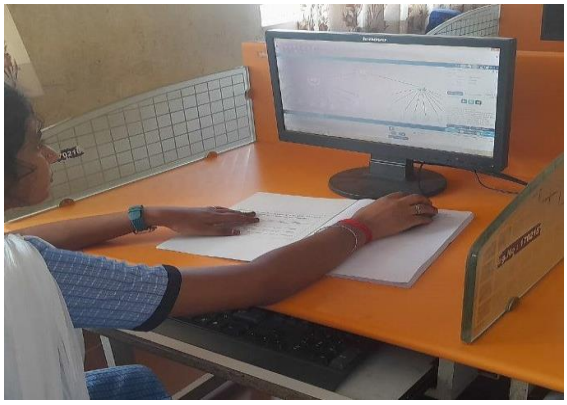
Our Department of Electronics and Communication Engineering successfully conducted a Four Day Value-Added Course on “System Verilog for Functional Verification: Concepts to Practice” for our third-year ECE Students handled by Resource Person Mr.V.Govindaraj, Intel Technology India Private Limited, Bangalore and Internal Faculty Members Ms.D.Ragavi, AP/ECE and Mrs.P.Nagarani Sobana, AP/ECE from 30.01.2025 to 02.02.2025. The course aimed to provide students with fundamental knowledge of digital design and verification methodologies and covered Verilog basics, System Verilog concepts, and hands-on sessions on functional verification.

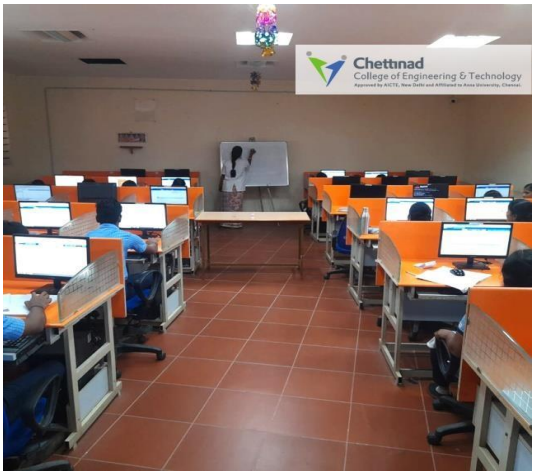




VALUE ADDED COURSE ON DESIGN A NETWORK IN CISCO PACKET TRACER

The Networks and Security subject activity titled “Design a network in Cisco Packet Tracer to connect ACCOUNTS and DELIVERY departments” was conducted for II ECE students on 07.03.2025. This practical session aimed to equip students with essential networking skills and knowledge required for designing and configuring computer networks.





GUEST LECTURES

Inauguration of ECE Department Association & Guest lecture on “Introduction to Microcontrollers”

The ECE Association Inauguration Function for the academic year 2024-2025 was held on the 27th of August 2024. The Chief Guest, Mr. Hareesh Janakiraman, Director of Embedded-Guru LLC, Houston, Texas, USA, highlighted the event with his lecture titled "Introduction to Microcontrollers”, and also interacted with the students and faculty members.

IEI STUDENT CHAPTER INAUGURATION OF ECE DEPARTMENT

The Student Chapter of the Institution of Engineers (India) for the departments of AI & DS, CSE, ECE, and EEE at Chettinad College of Engineering and Technology, Puliyur, Karur, was successfully inaugurated on Friday, 31st January 2025, in the presence of student members, faculty, and staff. The inauguration was graced by Dr. S. Dharmalingam, Former General Manager, BHEL, Trichy, Council Member, and Chairman, CCC, IEI,

who formally inaugurated the Student Chapter. In his inaugural address, he encouraged students to actively participate in the various activities planned under the chapter. The event was Presided by Dr. (Mrs.) A. Punitha, Principal, and was organized by Mr. B. Sathishkumar, Head-Admin, and was coordinated by Dr. M. Kumar, HoD/ECE. A total of 231 students, faculty members, and non-teaching staff attended the function, contributing to its grand success.

TECHNICAL EVENTS

BOOK FREE DAY

The Department of Electronics and Communication Engineering hosted a “BOOK FREE DAY” on September 13, 2024. This day was a grand combination of technical, non-technical, and poster-making competitions aimed at providing a comprehensive platform for intellectual exploration and skill enhancement.

The “TECHKRITI ‘2K24” poster making competition contest was conducted for our II, III and IV ECE students on September 13, 2024. All the teams enthusiastically took part in the contest and showed their hidden talent and thinking. The Poster Making Competition titled "Innovation in Electronics” to

encourage creativity and innovative thinking among students. Participants were tasked with designing posters that showcased new ideas, advancements, and creative concepts in the field of electronics, ranging from futuristic technologies to improvements in current systems.

BOOK FREE DAY (I ECE)

The Department of Electronics and Communication Engineering hosted a “BOOK FREE DAY” on November 25, 2024. This day was a grand amalgamation of technical and non-technical events aimed at providing a comprehensive platform for intellectual exploration and skill enhancement.

The “Bidyut 2K24” technical contest was conducted for our First Year ECE students on 25.11.2024. All the teams enthusiastically took part in the contest and showed their hidden talent and teamwork. The objective of this event is to foster skill development, encourage teamwork, promote creativity, provide stress relief and build a sense of community. The event focuses on enhancing soft skills, personality development and talent recognition while offering participants a platform to engage and have fun beyond their routine activities.

PEEK AND SEEK

On 26.09.2024, PEEK AND SEEK, a non–technical activity was organized for the first-year students. This activity enabled the students to learn new words and to improve their vocabulary and the art of learning new technical words and its spelling, meaning and pronunciation.

TECHTRIX’2025

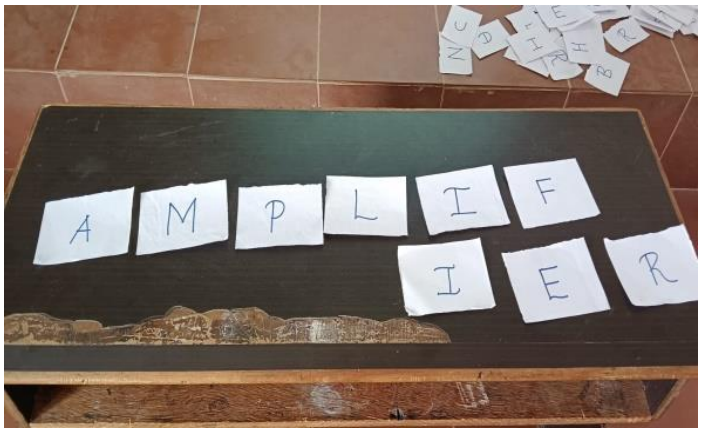
The Department of Electronics and Communication Engineering successfully organized a technical event, “TECHTRIX’2025”, to encourage critical thinking, improve communication skills, and promote healthy competition.

PRAGYA UTSA’2K25

The Department of Electronics and Communication Engineering successfully organized a technical event, “PRAGYA UTSAV ’2K25”,on 26.04.2025 for I-year students. The activity also aimed to recognize and reward students' participation, performance, and potential through certificates and appreciation, fostering a culture of excellence and innovation.

ELECTRONIKA'2K25

The "ELECTRONIKA '2K25" technical contest was conducted for our ECE students on 17.04.2025 All the teams enthusiastically took part in the contest and showed their hidden talent and thinking. This event helps the students to promote technical learning, problem-solving, and creativity in an engaging and competitive setting.



FUTURISTIC FRAMES 2K25

The Department of Electronics and Communication Engineering successfully organized a technical event, "The Futuristic Frames 2K25" – (Poster Design Contest) was conducted for II, III& IV ECE students on 01.04.2025. The main motto of conducting this activity for the students was to encourage and motivate them to develop and cultivate their thinking abilities, creativity, time management skills and presence of mind. The

students also actively participated in the contest and showcased their talent with their different creative and innovative ideas. This contest also promoted healthy competition, motivating students to challenge themselves and strive for excellence. Ultimately, this initiative aimed to recognize and reward outstanding creativity, acknowledging the efforts of participants through certificates, prizes, and public appreciation.

TECH TALKS

The "TECH TALKS" group discussion contest was conducted for our Second and Third Year ECE students on March 04, 2025. The purpose of this contest is to encourage students to explore cutting-edge advancements in technology. The event fosters collaboration, encourages knowledge-sharing, and inspires creative thinking by featuring insightful presentations, panel discussions, and interactive sessions. The goal of Fusion of Minds is to ignite innovative ideas, bridge knowledge gaps, and empower participants with actionable insights to drive technological progress.

This event tests the ability of participants to share their ideas about how AI-powered tools can support students with disabilities through speech-to-text, text-to-speech, and personalized learning aids. Participants are required to give their views about the benefits of AI in education

15 Teams (60 Students) participated in the Event 1-Group discussion. The top five teams were shortlisted for Round 2.

5 Teams (20 Students) were participated in the Event 2- Spot Topic.

GROUP DISCUSSION

SPOT TOPIC

This event helps the students increase their communication skills. Students were randomly assigned on-the-spot topics related to technology, social issues, or current affairs. Each group summarized and presented the key points of their discussion. Each group was given 2 minutes to gather their thoughts and plan their discussion. Groups engaged in active discussions, presenting their viewpoints, arguments, and counterarguments. Each group summarized and presented the key points of their discussion. 5 Teams (20 Students) participated in the Event 2-Spot Topic. The top 2 teams were awarded as Winners and Runners of the competition.

INNOVATION PITCH'2025

The Department of Electronics and Communication Engineering organized an intra-departmental event titled "Innovations Pitch" 2025 (Paper Presentation) on 5th May 2025, for II, III & IV Year ECE students. This event was designed to foster innovation, critical thinking, and communication skills among budding engineers by providing them a platform to present their research-based ideas in the field of Electronics. The session began with a warm welcome address delivered by a student representative, setting a dynamic tone for the event. The presentations showcased a wide range of innovative topics, including sustainable electronic design, wearable health devices, IoT applications, and circuit optimization. Students were evaluated on originality, clarity, practical application, and their ability to handle questions from the judging panel. Papers were submitted in IEEE format to the designated email ID (eceinnovationspitch@gmail.com). Each team was allotted 5 minutes for presentation followed by a 1–2 minute Q&A session. This event was evaluated by Mr.Senthilkumar, Professor /EEE and Mrs.J.Jenisha, AP/ECE.

INDUSTRIAL VISIT

On the 18th and 19th of April 2025, students from the Electronics and Communication Engineering Department (I, II, III, and IV Years) participated in an industrial visit organized to enhance their practical understanding of industry operations. A total of 105 students, accompanied by 6 faculty members, visited three key locations: Traco Cable Company in Kochi, Marayoor Jaggery Production Unit in Marayoor, and Wonderla Amusement Park in Kochi.

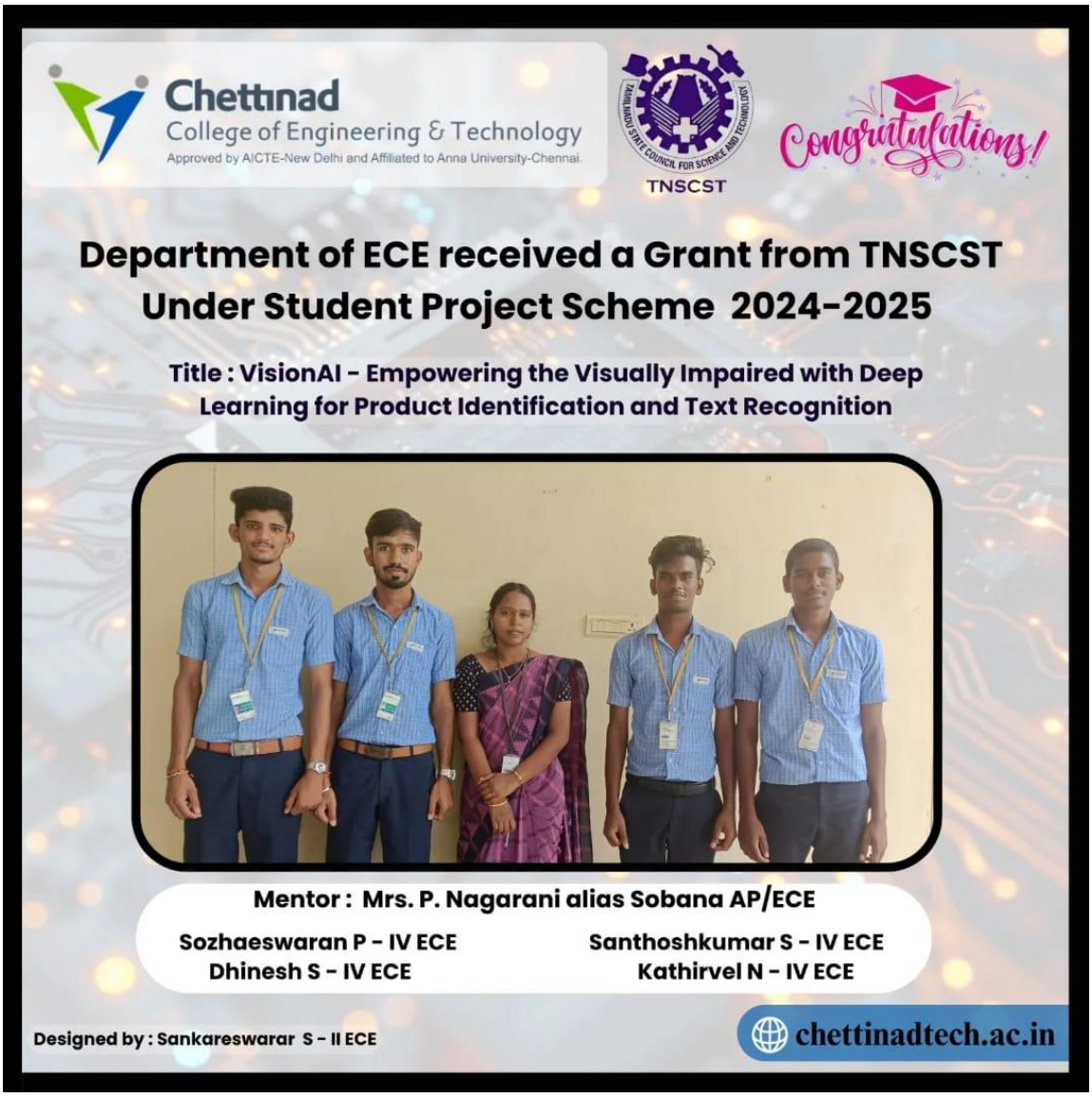
STUDENTS ACHIEVEMENTS & PARTICIPATIONS

NIRAL THIRUVIZHA2.0 – A STATE LEVEL PROJECT CONTEST ORGANISED BY TAMILNADU SKILL DEVELOPMENT CORPORATION

- ✓ Our Final Year ECE students actively participated in Naan Mudhalvan Niral Thiruvizha 2.0, and three teams were selected for the final round, winning a cash prize of ₹10,000 each.

TNSCST STUDENT PROJECT SCHEME

- ✓ A project idea from the ECE department has been selected by TNSCST. The project, titled 'Vision AI: Empowering the Visually Impaired with Deep Learning for Product Identification and Text Recognition,' was proposed by our final year students P. Sozhaeswarn, S. Santhoshkumar, S. Dhinesh, N. Kathrivel.



NPTEL ACHIEVEMENTS

Several students from the IV, III and II year batches have successfully completed NPTEL certification courses conducted by premier institutions like IIT Guwahati, IIT Kharagpur, IIT Bombay, IIT Roorkee, and IGNOU. The courses covered diverse areas such as System Design through Verilog, Programming in Java, Microprocessors and Microcontrollers, VLSI Design, Introduction to IOT and Cloud Computing. A significant number of students have earned Elite and Elite + Silver certifications, reflecting their strong academic performance. Most of these courses ranged from 4 to 12 weeks in duration and were held between July 2024 and April 2025. This achievement demonstrates the students' dedication to enhancing their technical skills beyond the regular curriculum. Such accomplishments also contribute to their academic growth and improve their future career opportunities.

S.No	Name of the Student	Year/ Sem	Name of the Course Registered	Organized by	Course Duration	Status
1	Abarna K	IV/VII	System Design Through Verilog	IIT Guwahati	8 Weeks Jul-Sep 2024	Successfully completed
2	Abirami M	IV/VII	System Design Through Verilog	IIT Guwahati	8 Weeks Jul-Sep 2024	Elite
3	Aravinth.S	IV/VII	System Design Through Verilog	IIT Guwahati	8 Weeks Jul-Sep 2024	Successfully completed
4	Bubalakannan.R	IV/VII	System Design Through Verilog	IIT Guwahati	8 Weeks Jul-Sep 2024	Elite +Silver
5	Dinesh B	IV/VII	System Design Through Verilog	IIT Guwahati	8 Weeks Jul-Sep 2024	Successfully completed

6	Jeevanantham R	IV/VII	System Design Through Verilog	IIT Guwati	8 Weeks Jul-Sep 2024	Elite
7	Kiran G	IV/VII	System Design Through Verilog	IIT Guwahati	8 Weeks Jul-Sep 2024	Elite +Silver
8	Manirathinam S	IV/VII	System Design Through Verilog	IIT Guwahati	8 Weeks Jul-Sep 2024	Elite +Silver
9	Naveenkumar S	IV/VII	System Design Through Verilog	IIT Guwahati	8 Weeks Jul-Sep 2024	Elite
10	Nishok Aananth.E	IV/VII	System Design Through Verilog	IIT Guwahati	8 Weeks Jul-Sep 2024	Elite +Silver
11	Nithishkumar.P	IV/VII	System Design Through Verilog	IIT Guwahati	8 Weeks Jul-Sep 2024	Elite
12	Raghul B	IV/VII	System Design Through Verilog	IIT Guwahati	8 Weeks Jul-Sep 2024	Elite +Silver
13	Santhoshkumar.S	IV/VII	System Design Through Verilog	IIT Guwahati	8 Weeks Jul-Sep 2024	Elite
14	Sozhaeswaran P	IV/VII	System Design Through Verilog	IIT Guwahati	8 Weeks Jul-Sep 2024	Elite
15	Abishek S	IV/VII	Google cloud computing foundations	IIT Kharagpur	8 weeks Aug-Oct 2024	Elite
16	Balamurugan K	IV/VII	Programming in modern c++	IIT Kharagpur	12 weeks Jul-Oct 2024	Successfully completed
17	Divya K	IV/VII	Programming in java	IIT Kharagpur	12 weeks Jul-Oct 2024	Successfully completed
18	Gowsalya B	IV/VII	Programming in Java	IIT Kharagpur	12 weeks Jul-Oct 2024	Elite
19	Harish R	IV/VII	Programming in Java	IIT Kharagpur	12 weeks Jul-Oct 2024	Successfully completed

20	Jeevitha M	IV/VII	Programming in Java	IIT Kharagpur	12 weeks Jul-Oct 2024	Successfully completed
21	Gunasekar.M	IV/VII	Web Technology	IGNOU-New Delhi	12 weeks Jul-Dec 2024	Successfully completed
22	Gayathri T	IV/VII	Web Technology	IGNOU-New Delhi	12 weeks Jul-Dec 2024	Successfully completed
23	Lavanya M	IV/VII	Web Technology	IGNOU-New Delhi	12 weeks Jul-Dec 2024	Successfully completed
24	Sibiraj R	IV/VII	Web Technology	IGNOU-New Delhi	12 weeks Jul-Dec 2024	Successfully completed
25	Varni S	IV/VII	Web Technology	IGNOU-New Delhi	12 weeks Jul-Dec 2024	Successfully completed
26	Abisekar P	IV/VII	System Design through Verilog	IIT Guwahati	8 Weeks Jul-Sep 2024	Elite
27	Santhanabharathi R	IV/VII	System Design through Verilog	IIT Guwahati	8 Weeks Jul-Sep 2024	Elite
28	Dharani K	IV/V	Software Conceptual Design	IIT- Bombay	4 Weeks Aug-Sep 2024	Elite
29	Pooja H	IV/V	Introduction to Internet of Things	IIT Kharagpur	12 Weeks Jul-Oct 2024	Elite
30	Poorva Sri P	IV/V	Introduction to Internet of Things	IIT Kharagpur	12 Weeks Jul-Oct 2024	Elite
31	Srinidhi R	IV/V	Digital VLSI Testing	IIT Kharagpur	12 Weeks Jul-Oct 2024	Successfully completed
32	Yuvashree N	IV/V	Digital VLSI Testing	IIT Kharagpur	12 Weeks Jul-Oct 2024	Successfully completed
33	Abisekar P	III/VI	VLSI Physical Design with Timing Analysis	IIT Roorkee	12 Weeks Jan-Apr 2025	Elite
34	Devasri S P	III/VI	Microprocessors and Microcontrollers	IIT Kharagpur	12 Weeks Jan-Apr 2025	Successfully completed

35	Dharani K	III/VI	Microprocessors and Microcontrollers	IIT Kharagpur	12 Weeks Jan-Apr 2025	Successfully completed
36	Dharanika R	III/VI	Microprocessors and Microcontrollers	IIT Kharagpur	12 Weeks Jan-Apr 2025	Successfully completed
37	Harisha V	III/VI	Microprocessors and Microcontrollers	IIT Kharagpur	12 Weeks Jan-Apr 2025	Elite
38	Harthika S	III/VI	Microprocessors and Microcontrollers	IIT Kharagpur	12 Weeks Jan-Apr 2025	Successfully completed
39	Jeevakarunya A	III/VI	Microprocessors and Microcontrollers	IIT Kharagpur	12 Weeks Jan-Apr 2025	Successfully completed
40	Kokila L	III/VI	Microprocessors and Microcontrollers	IIT Kharagpur	12 Weeks Jan-Apr 2025	Elite
41	Logesh S	III/VI	VLSI Physical Design with Timing Analysis	IIT Kharagpur	12 Weeks Jan-Apr 2025	Successfully completed
42	Mathan Raj S	III/VI	Microprocessors and Microcontrollers	IIT Kharagpur	12 Weeks Jan-Apr 2025	Elite
43	Mathumitha M	III/VI	Microprocessors and Microcontrollers	IIT Kharagpur	12 Weeks Jan-Apr 2025	Successfully completed
44	Navin S	III/VI	Microprocessors and Microcontrollers	IIT Kharagpur	12 Weeks Jan-Apr 2025	Successfully completed
45	Piragadeesh TM	III/VI	Microprocessors and Microcontrollers	IIT Kharagpur	12 Weeks Jan-Apr 2025	Successfully completed
46	Pooja H	III/VI	Microprocessors and Microcontrollers	IIT Kharagpur	12 Weeks Jan-Apr 2025	Elite
47	Poorva Sri P	III/VI	Microprocessors and Microcontrollers	IIT Kharagpur	12 Weeks Jan-Apr 2025	Successfully completed
48	Pradeep C	III/VI	Microprocessors and Microcontrollers	IIT Kharagpur	12 Weeks Jan-Apr 2025	Successfully completed
49	Pravin kumar S	III/VI	Microprocessors and Microcontrollers	IIT Kharagpur	12 Weeks Jan-Apr 2025	Elite

50	Priya Dharshini G	III/VI	Microprocessors and Microcontrollers	IIT Kharagpur	12 Weeks Jan-Apr 2025	Successfully completed
51	Rithika B	III/VI	Programming In Java	IIT Kharagpur	12 Weeks Jan-Apr 2025	Elite
52	Sandhiya S	III/VI	Microprocessors and Microcontrollers	IIT Kharagpur	12 Weeks Jan-Apr 2025	Successfully completed
53	Veena R	III/VI	Microprocessors and Microcontrollers	IIT Kharagpur	12 Weeks Jan-Apr 2025	Successfully completed
54	Yuvashree M	III/VI	Microprocessors and Microcontrollers	IIT Kharagpur	12 Weeks Jan-Apr 2025	Successfully completed
55	Yuvashree N	III/VI	Microprocessors and Microcontrollers	IIT Kharagpur	12 Weeks Jan-Apr 2025	Elite
56	Prakash.B	II/IV	Introduction to IOT	IIT Kharagpur	12 Weeks Jan-Apr 2025	Elite +Silver

SPORTS ACHIEVEMEN

Chettinad Tech 17th Annual Sports Day Highlights!

Our campus was alive with energy and excitement on May 3rd, 2025, as we celebrated the 17th Sports Day in full spirit!

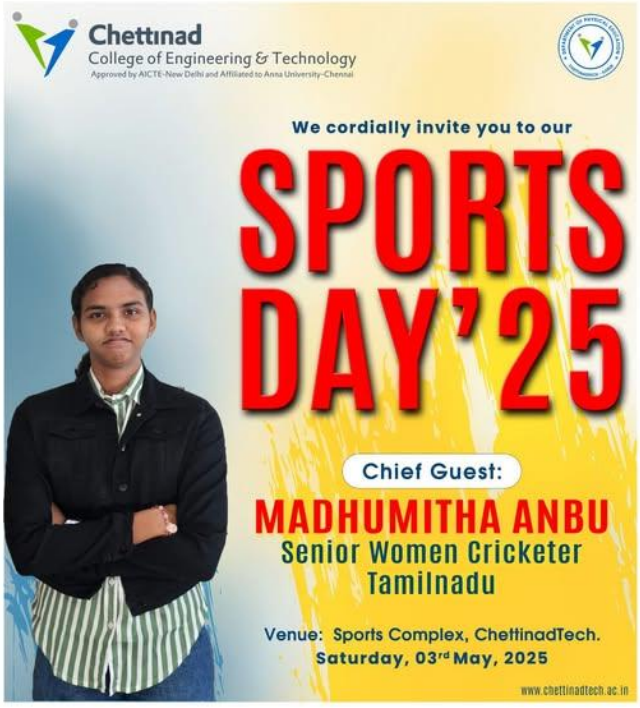
From the grand flag hoisting and disciplined march-past by all departments to exhilarating sports events, cultural performances, and even pyramid formations—our students truly showcased teamwork and talent.

Special thanks to our Chief Guest, Ms. A. Madhumitha Anbu, Tamil Nadu Cricket Player, for inspiring us with her presence!

Faculty also joined in the fun with events like “Try Your Luck” and “Tug of War”!

Kudos to the ECE Department for winning the Overall Championship!

A big shoutout to all the participants, organizers, and supporters who made the day unforgettable!


Chettinad
College of Engineering & Technology
Approved by AICTE-New Delhi and Affiliated to Anna University-Chennai
We cordially invite you to our
SPORTS DAY'25
Chief Guest:
MADHUMITHA ANBU
Senior Women Cricketer
Tamilnadu
Venue: Sports Complex, ChettinadTech.
Saturday, 03rd May, 2025
www.chettinadtech.ac.in


Chettinad
College of Engineering & Technology
Approved by AICTE, New Delhi and Affiliated to Anna University, Chennai.

INTERNSHIPS

In the academic year 2024–2025, our Final Year and Third Year ECE students secured internships in various reputed companies, gaining valuable industry exposure and hands-on experience in core and interdisciplinary domains. The details of the internships are listed below:

NAME OF THE COMPANY		NO. OF STUDENTS
TESSOLVE A HERO ELECTRONIX VENTURE	Tessolve Semiconductor Pvt Ltd	02
Delphi – TVS Technologies	M/S Delphi-TVS Technologies Ltd	10
MITSUBA	Mitsuba India Pvt Ltd	07
FOXCONN	Foxconn India Private Ltd	05
SiMaxTech Silicon Innovation at Max	SiMax Tech Private Ltd	02
TVS UPASANA LTD	TVS Upasana Ltd	06
motherson sumi systems limited	Motherson Sumi Wiring India Ltd	04
WE TOUCH TECHNOLOGIES	We Touch Technologies	01
Celebration of life	Celebration of Life	01

ILIFE TECHNOLOGIES	I Life Technology	01
TARAS SYSTEMS AND SOLUTIONS	Taras Systems and Solutions	09
YAMAHA Make Waves	Yamaha Music India Pvt Ltd	08

PLACEMENTS (2024-25)

In this academic year, our Final Year ECE students have successfully secured placements in reputed companies across various domains. The consistent placement performance showcases the department's commitment to excellence in education and skill development.

NAME OF THE COMPANY		NO. OF STUDENTS
TESSOLVE A HERO ELECTRONIX VENTURE	Tessolve Semiconductor Pvt Ltd	02
Delphi – TVS Technologies	M/S Delphi-TVS Technologies Ltd	10
MITSUBA	Mitsuba India Pvt Ltd	07
FOXCONN	Foxconn India Private Ltd	05
SiMaxTech Silicon Innovation at Max	SiMax Tech Private Ltd	02
TVS UPASANA LTD	TVS Upasana Ltd	06

	Motherson Sumi Wiring India Ltd	04
	We Touch Technologies	01
	Celebration of Life	01
	I Life Technology	01
	Taras Systems and Solutions	09
	Yamaha Music India Pvt Ltd	08
	KGiSL Technologies	02

FACULTY CONTRIBUTIONS

Dr. M. Kumar

- ✓ **Kumar.M,** Abishek.S, Jeevanantham.R, Kiran.G, Thiyagarajan.S, **"Detecting Diabetic Retinopathy Using Image Processing"** International Journal Of Scientific Research In Engineering And Management, Vol. 9 (5), May 2025.
- ✓ **Kumar.M, "Dual-Mode Fluorescent and Colorimetric Sensors Powered by Machine Learning for High-Security Authentication and Anti-Counterfeiting"**. 2024 IEEE 9th International Conference on Engineering, Technologies & Applied Sciences (ICETAS 2024), December 2024.

- ✓ A. Bala Ayyappan, T. Gobinath, **M. Kumar**, A. Sivaramakrishnan, **"Rice Plant Disease Detection using Convolutional Neural Networks",** Discover Artificial Intelligence 5, 50 (2025).
- ✓ A. Bala Ayyappan, T. Gobinath, **M. Kumar**, A. Sivaramakrishnan, "**Predicting Monsoon Variability in Erode and Trichy: A Data-Driven Approach Using Machine Learning**", 4th International Conference on Deep sciences for computiung and communications, April 2025.

Mr. P. Selvan

- ✓ Participated in and successfully completed the **AICTE Training and Learning (ATAL)** Academy FDP on "**Quantum Neuromorphic Computing for Viable and Sustainable Generative AI**", held from 2nd to 7th December 2024 at M. Kumarasamy College of Engineering.
- ✓ Attended a **one-day Entrepreneurship Awareness Programme** organized by the **DIC Office, Karur** at the **National level**.
- ✓ Attended the **FDP on "Artificial Intelligence for 5G/6G Communication Systems and Signal Processing Applications"** conducted from **19th to 29th May 2025** at M. Kumarasamy College of Engineering.
- ✓ Published a research paper titled "**Optimizing Brain Tumor Classification: A Comparative Analysis of Nature-Inspired Algorithms with GLCM Features**" (co-authored with Kavitha A. and Ragul S.) published in the **journal Biomedical Materials and Devices (International level)**.
- ✓ Published a research paper titled "**Hybrid CNN-BI-LSTM Network for the Accurate Brain Tumour Prediction in MRI Image**" (co-authored with Kavitha A., Karthic Kumar V., Kavitha V., and Yahini A.) and presented at the **GINOTECH 2025 Conference (IEEE, National level)**.

- ✓ Presented a paper titled "**Smart IoT Based Robotic Surveillance System**" (co-authored with Sozhaeswaran P., Dhinesh S., Santhoshkumar S., and Kathirvel N.) at the **16th ICCCNT Conference (IEEE, National level)**.
- ✓ Published a research paper titled "**Smart Fish Aquaculture Monitoring System**" (co-authored with E. Nishok Aananth, S. Aravinth, B. Dinesh, and K. Ponthiruselvam) in the **International Journal of Innovative Research in Technology**.

Ms. D. Ragavi

- ✓ Participated in the international training program on "**Smart System Integration with Wireless Sensors**" organized by NITTTR, Chandigarh from **August 5 to 9, 2024**.
- ✓ Attended the international training on "**Microstrip Patch Antenna Design Techniques and Tools**" organized by NITTTR, Chandigarh from **September 16 to 20, 2024**.
- ✓ Attended the international training program on "**Teaching ECE Lab Subjects Using Free Simulators**" organized by NITTTR, Chandigarh from **March 3 to 7, 2025**.

Mr. M. Prabhakaran

- ✓ Published a research paper titled "**An Improved Face Image Restoration Method Based on Denoising Diffusion Probabilistic Models**" in an **International Journal at the IJRAR publication event** on **19th May 2025**.
- ✓ Published a paper titled "**Human Presence Identifier in Landslide Zones**" in an **International Journal at IJRAR publication event** held on **19th May 2025**.
- ✓ Successfully completed the **Microsoft Digital Skilling Program** under the **Naan Mudhalvan initiative,** earning an 'A' grade in **2024**.

- ✓ Published a research paper titled "**Energy Efficient Multimedia Transmission in Wireless Sensor Networks using Enhanced Adaptive Transmission Control Algorithm and Measurement Techniques**" on 3rd December 2024.

Mrs. A. Karthikeyani

- ✓ Participated in the international training program on "**Smart System Integration with Wireless Sensors**" organized by NITTTR, Chandigarh from **August 5 to 9, 2024**.
- ✓ Attended the international training on "**Microstrip Patch Antenna Design Techniques and Tools**" organized by NITTTR, Chandigarh from **September 16 to 20, 2024**.
- ✓ Attended the international training program on "**Teaching ECE Lab Subjects Using Free Simulators**" organized by NITTTR, Chandigarh from **March 3 to 7, 2025**.

Mr. M. Mohanraj

- ✓ Published a paper titled "**An Improved Face Image Restoration Method Based on Denoising Diffusion Probabilistic Models**" in an **International Journal at IJRAR publication event** held on **19th May 2025**.

Dr. M. Mahesh

- ✓ Published a paper titled "**AI Based Liver Tissue Prediction Using CNN Algorithm**" in an **International Journal at IJRAR** publication event held on **19th May 2025**.

Mrs. P. Nagarani alias Sobana

- ✓ Presented a paper titled "**IoT-Based Early Flood Detection and Avoidance**" at the **ICETET'25** conference held on **April 4th and 5th, 2025**.

- ✓ Attended the international training program on "**Teaching ECE Lab Subjects Using Free Simulators**" organized by NITTTR, Chandigarh from **March 3 to 7, 2025**.

Ms. J. Jenisha

- ✓ Published a research paper titled **"Textile Substrate Materials for Wearable Antenna Applications: A Review"** (co-authored with M. Manikandan, P. Rajasekaran, V. Srinath, V. Femina) in the 10th International Conference on Advanced Computing and Communication Systems (ICACCS) ISBN: 979-8-3503-8436-9 | Pages: 611–617 (IEEE Xplore) | DOI: 10.1109/ICACCS60874.2024.10716910
- ✓ Successfully completed the "**EBPL-Software for Products"** course with A+ grade under the **Naan Mudhalvan Program** held at Anna University, Madurai from **February 10 to 16, 2025**.
- ✓ Attended the international training program on "**Teaching ECE Lab Subjects Using Free Simulators**" organized by NITTTR, Chandigarh from **March 3 to 7, 2025**.
- ✓ Presented a paper titled **"AR based learning and Career Guidance Platform"** in the International Conference on Recent Trends in Technology **"ICRTT - 2k25"** held on **2nd May 2025** at Nadar Saraswathi College of Engineering and Technology, Theni.

Mr. M. Pradeepraj

- ✓ Attended the **Faculty Development Programme on "Intelligent IoT Computing"** from **3rd to 8th February 2025** in Coimbatore.
- ✓ Participated in the FDP on "**ADAS ECU Simulation and Testing**" conducted from **10th to 16th February 2025** at Government College of Engineering, Srirangam.
- ✓ Published a paper titled "**Design a Smart Helmet with Multi-Fusion Sensor for Accident Detection**" in an **International Journal (IJSREM)** on **19th May 2025**

Editorial Board

Faculty Members

1. Mr.P.Selvan, ASP/ECE
2. Mrs.A.Karthikeyani, AP/ECE

Student Members

1. M.Arsath Ansari, III ECE
2. S.Mathanraj, III ECE
3. S.Sankareswarar, II ECE
4. N.Hiriseeka, II ECE